



# MS-7501 VER:1.0

## CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

## System Chipset:

AMD/ATI RS780

AMD/ATI SB700

## On Board Chipset:

FINTEK Super I/O -- F71882

LAN -- RTL8111C(B)/RTL8101E

HD Codec -- ALC888

BIOS -- SPI ROM 8M

1394 -- JMB381

## Main Memory:

DDR II X 4 (Max 8GB)

## Expansion Slots:

PCI-E X 16 \*1

PCI-E X 1 \*1

PCI 2.2 Slot X 2

## Clock Generator:

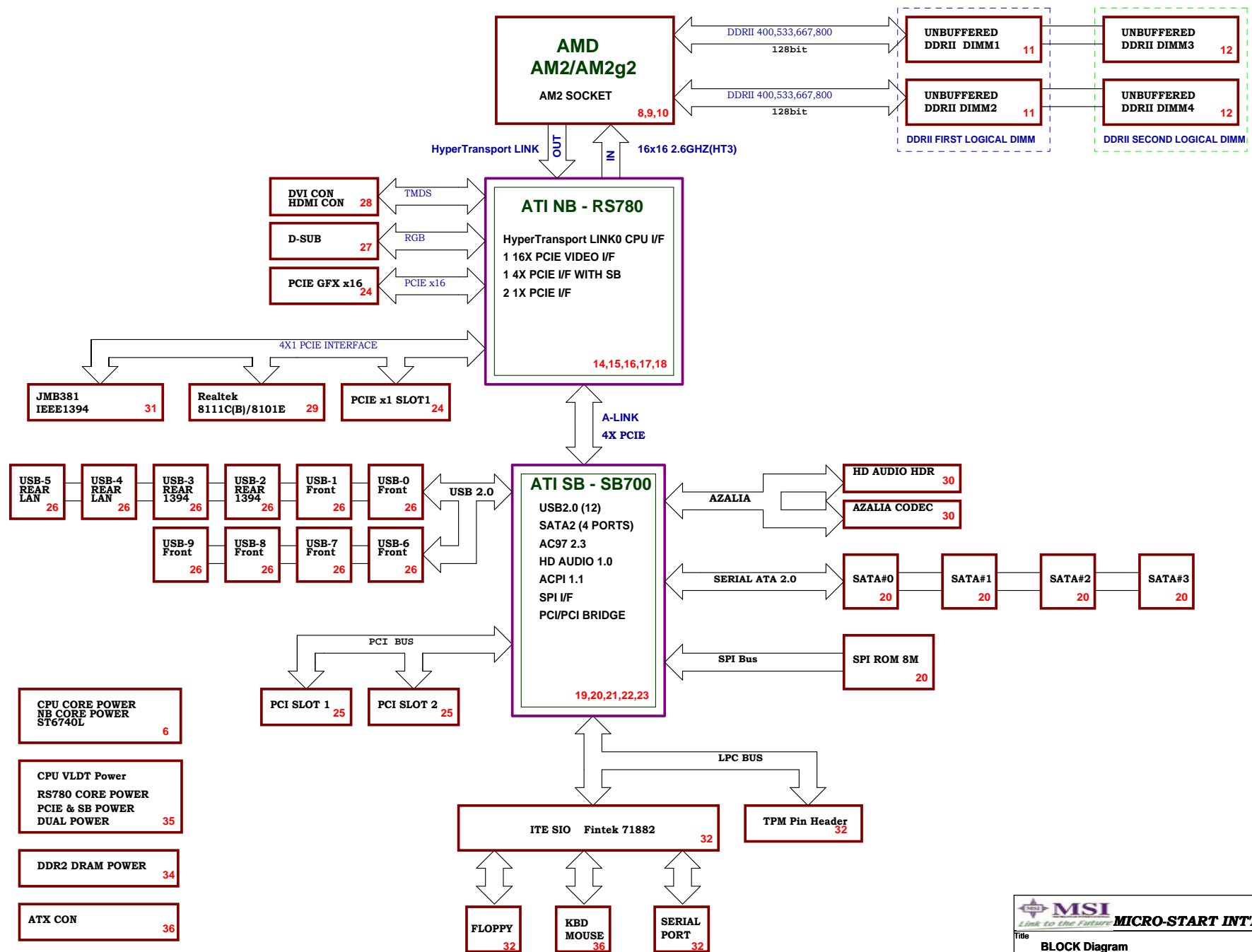
Controller--ICS9LPRS477

## PWM:

Controller -- ST6740L + UP6262 3+1 Phase

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# Project RS-780 BLOCK DIAGRAM



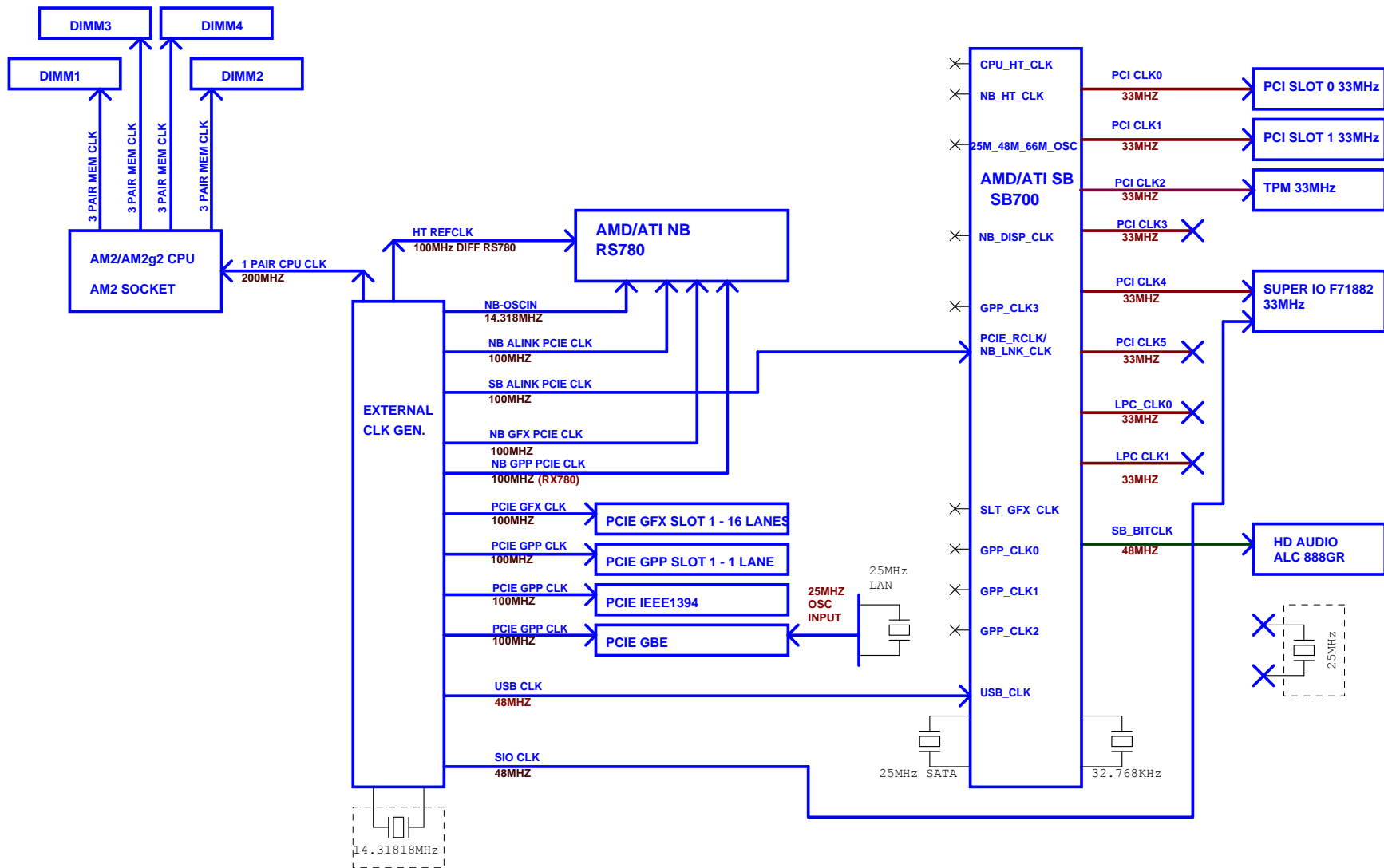
GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RI#/EXTENVNT0#		RI#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SM#/#EXTENVNT1#		LPC_SM#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

[illegible]

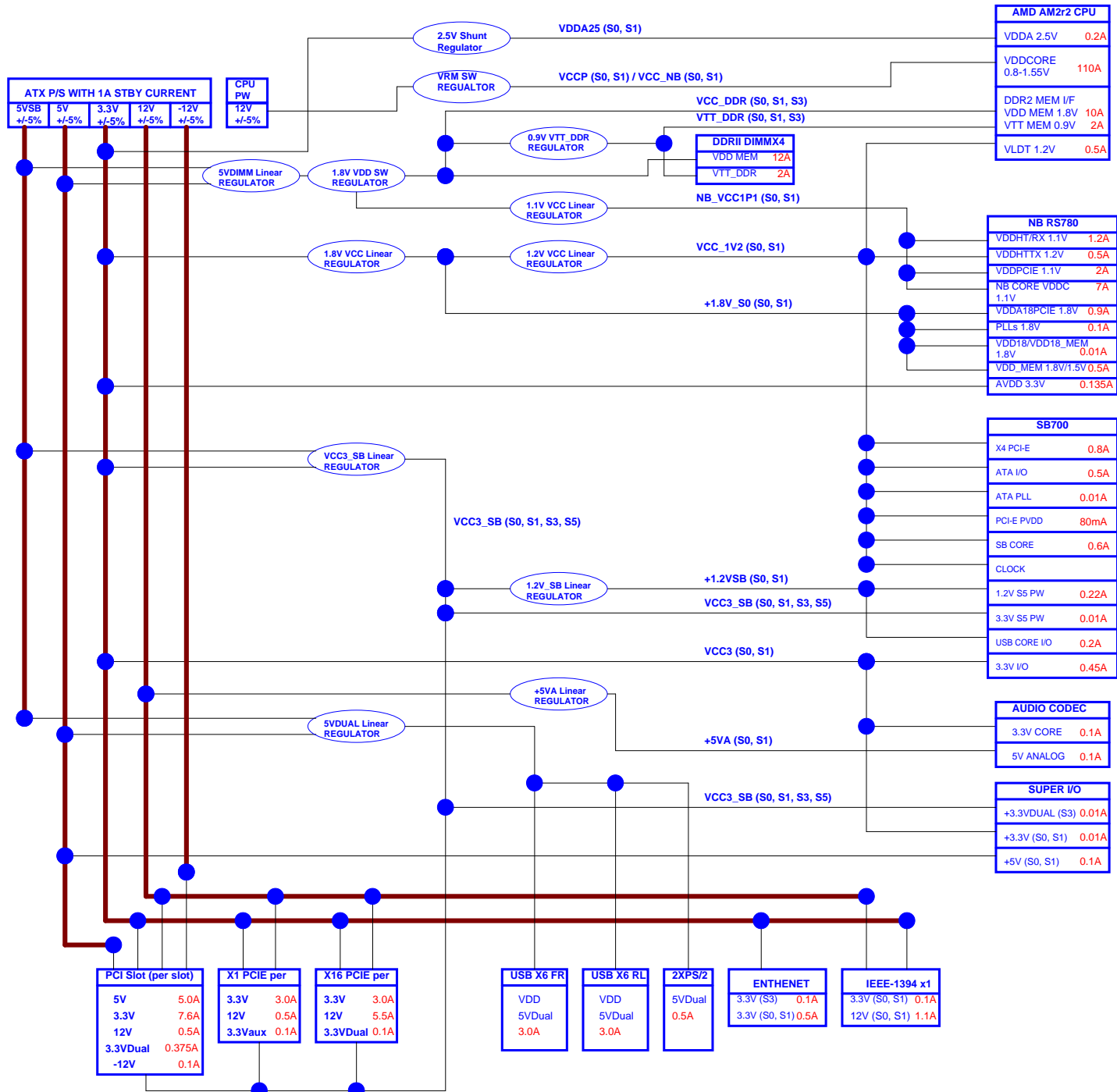
GPIO Name	Type	Function Description	Pin	Page
VIDO5/GP27		LEO_GPIO2	20	26
VIDO4/GP26		LEO_GPIO1	21	26
VIDO1/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SM#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SS_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

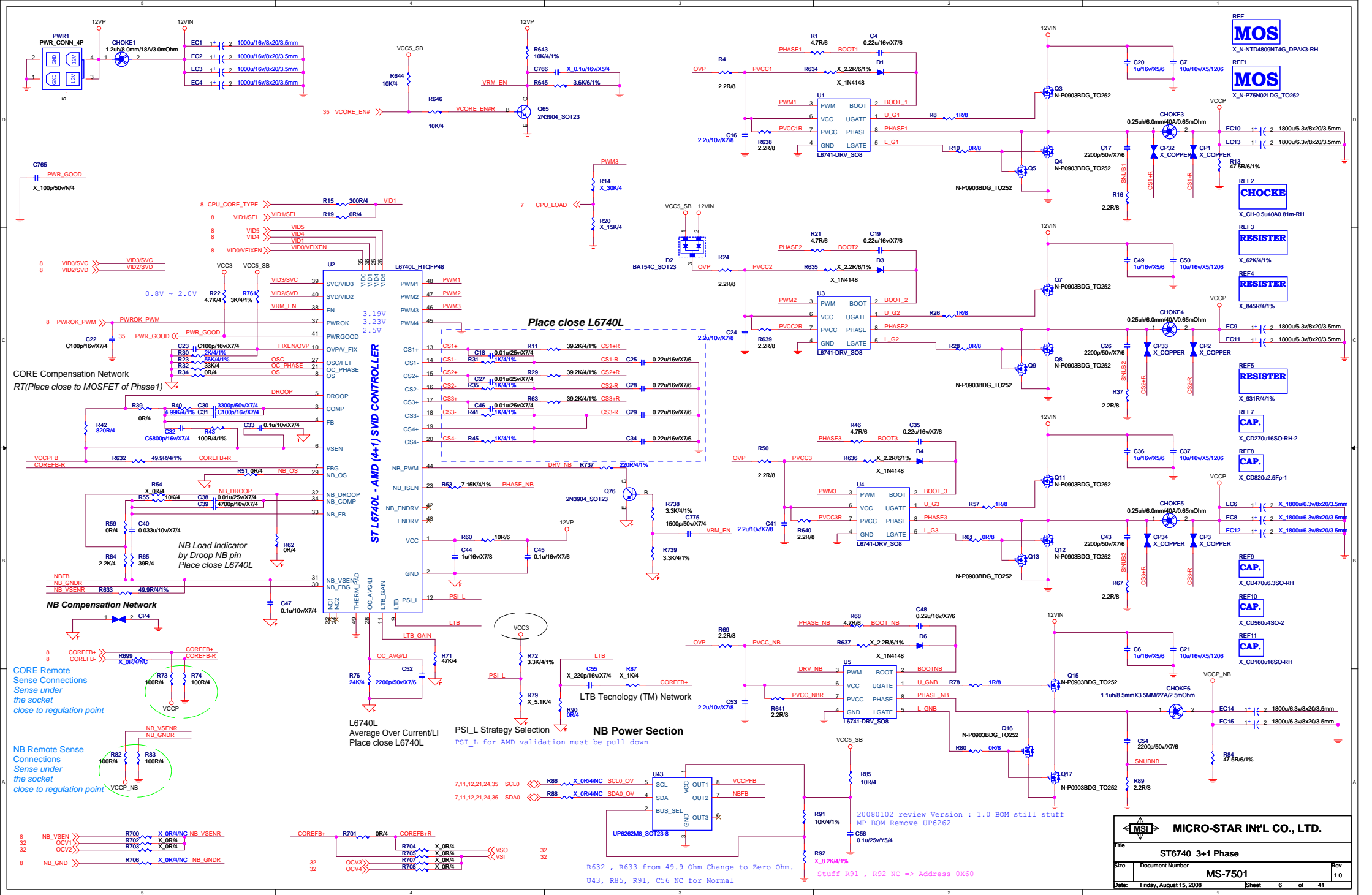
DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTE# PCI_INTF# PCI_INTG# PCI_INTH#	PREQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTF# PCI_INTG# PCI_INTH# PCI_INTE#	PREQ#1 PGNT#1	AD22	PCICLK1

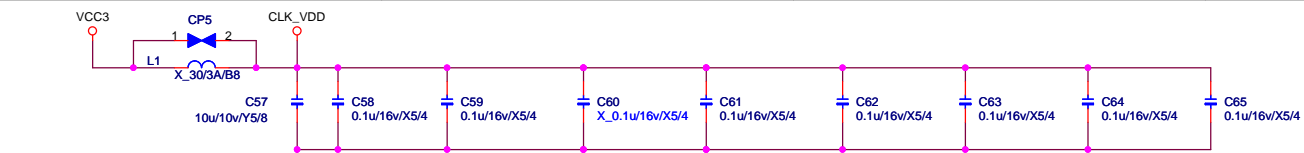


External clock mode  
Internal clock mode

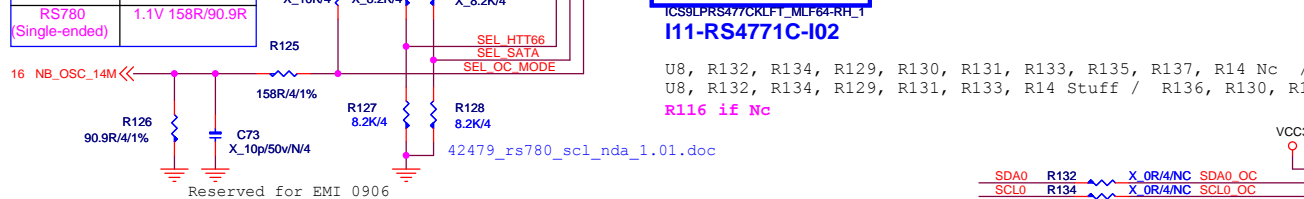
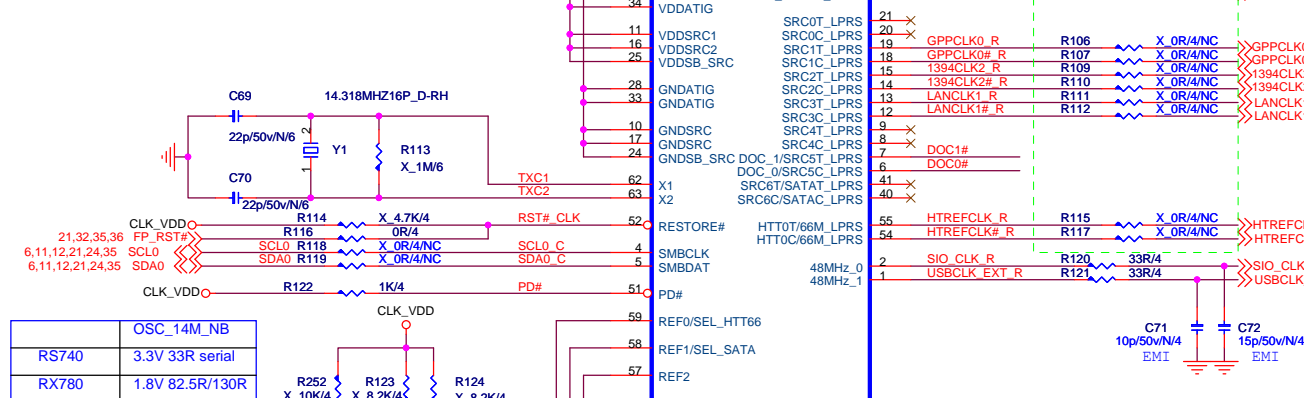
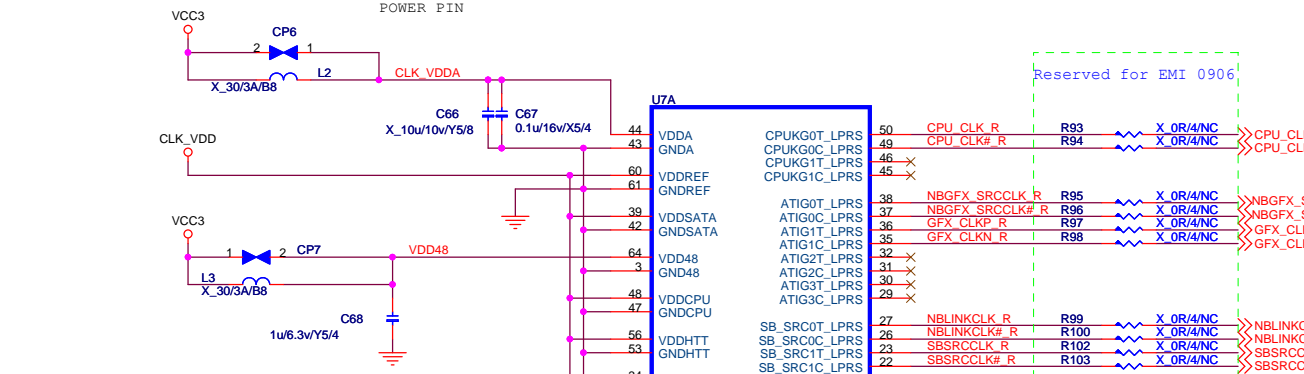
Power Deliver Chart







- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U41 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U41 POWER PIN

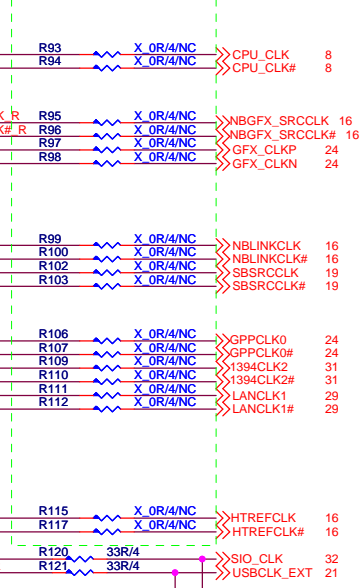


REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

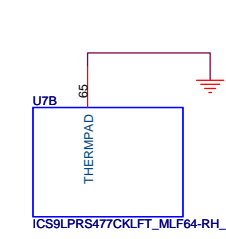
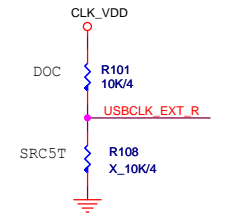
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

EXT CLK FREQUENCY SELECT TABLE(MHZ)

Reserved for EMI 0906

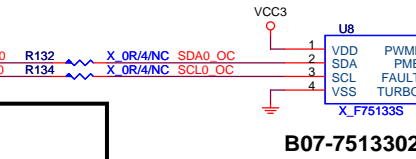


SB700 Pin C8 USBCLK/14M\_25M\_48M\_OSC Function set output pin by BIOS.



I11-RS4771C-I02

U8, R132, R134, R129, R130, R131, R133, R135, R137, R14 Nc / R136 Stuff  
U8, R132, R134, R129, R131, R133, R14 Stuff / R136, R130, R135, R137 Nc  
R116 if Nc



B07-7513302-F34

Micro Star Restricted Secret		
Title	Clock-Gen ICS9LPRS477	Rev
Document Number	MS-7501	1.0
MICRO STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, August 15, 2008
Sheet		7 of 40







11,12 MEM\_MA\_DQS\_L[7..0] >> MEM\_MA\_DQS\_L[7..0]  
11,12 MEM\_MA\_DQS\_H[7..0] >> MEM\_MA\_DQS\_H[7..0]  
11,12 MEM\_MA\_DM[7..0] >> MEM\_MA\_DM[7..0]  
11,12,13 MEM\_MA\_ADD[15..0] >> MEM\_MA\_ADD[15..0]  
11,12 MEM\_MA\_DATA[63..0] >> MEM\_MA\_DATA[63..0]

11,12 MEM\_MB\_DQS\_L[7..0] >> MEM\_MB\_DQS\_L[7..0]  
11,12 MEM\_MB\_DQS\_H[7..0] >> MEM\_MB\_DQS\_H[7..0]  
11,12 MEM\_MB\_DM[7..0] >> MEM\_MB\_DM[7..0]  
11,12,13 MEM\_MB\_ADD[15..0] >> MEM\_MB\_ADD[15..0]  
11,12 MEM\_MB\_DATA[63..0] >> MEM\_MB\_DATA[63..0]

CPU1B

MEMORY INTERFACE A

11,13 MEM_MA0_CLK_H2	>>	MEM_MA0_CLK_H2	AG21	MA0_CLK_H(2)	MA_DATA(63)
11,13 MEM_MA0_CLK_L2	>>	MEM_MA0_CLK_L2	AG20	MA0_CLK_L(2)	MA_DATA(62)
11,13 MEM_MA0_CLK_H1	>>	MEM_MA0_CLK_H1	G19	MA0_CLK_H(1)	MA_DATA(61)
11,13 MEM_MA0_CLK_L1	>>	MEM_MA0_CLK_L1	H19	MA0_CLK_L(1)	MA_DATA(60)
11,13 MEM_MA0_CLK_H0	>>	MEM_MA0_CLK_H0	U27	MA0_CLK_H(0)	MA_DATA(59)
11,13 MEM_MA0_CLK_L0	>>	MEM_MA0_CLK_L0	U26	MA0_CLK_L(0)	MA_DATA(58)
11,13 MEM_MA0_CS_L1	>>	MEM_MA0_CS_L1	AC25	MA0_CS_L(1)	MA_DATA(57)
11,13 MEM_MA0_CS_L0	>>	MEM_MA0_CS_L0	AA24	MA0_CS_L(0)	MA_DATA(56)
11,13 MEM_MA0_ODT0	>>	MEM_MA0_ODT0	AC28	MA0_ODT(0)	MA_DATA(54)
12,13 MEM_MA1_CLK_H2	>>	MEM_MA1_CLK_H2	AE20	MA1_CLK_H(2)	MA_DATA(53)
12,13 MEM_MA1_CLK_L2	>>	MEM_MA1_CLK_L2	AE19	MA1_CLK_L(2)	MA_DATA(52)
12,13 MEM_MA1_CLK_H1	>>	MEM_MA1_CLK_H1	G20	MA1_CLK_H(1)	MA_DATA(51)
12,13 MEM_MA1_CLK_L1	>>	MEM_MA1_CLK_L1	G21	MA1_CLK_L(1)	MA_DATA(50)
12,13 MEM_MA1_CLK_H0	>>	MEM_MA1_CLK_H0	V27	MA1_CLK_H(0)	MA_DATA(49)
12,13 MEM_MA1_CLK_L0	>>	MEM_MA1_CLK_L0	W27	MA1_CLK_L(0)	MA_DATA(48)
12,13 MEM_MA1_CS_L1	>>	MEM_MA1_CS_L1	AD27	MA1_CS_L(1)	MA_DATA(47)
12,13 MEM_MA1_CS_L0	>>	MEM_MA1_CS_L0	AA25	MA1_CS_L(0)	MA_DATA(46)
12,13 MEM_MA1_ODT0	>>	MEM_MA1_ODT0	AC27	MA1_ODT(0)	MA_DATA(45)
11,12,13 MEM_MA_CAS_L	>>	MEM_MA_CAS_L	AB25	MA_CAS_L	MA_DATA(44)
11,12,13 MEM_MA_WE_L	>>	MEM_MA_WE_L	AB27	MA_WE_L	MA_DATA(43)
11,12,13 MEM_MA_RAS_L	>>	MEM_MA_RAS_L	AA26	MA_RAS_L	MA_DATA(42)
11,12,13 MEM_MA_BANK2	>>	MEM_MA_BANK2	N25	MA_BANK(2)	MA_DATA(41)
11,12,13 MEM_MA_BANK1	>>	MEM_MA_BANK1	Y27	MA_BANK(1)	MA_DATA(40)
11,12,13 MEM_MA_BANK0	>>	MEM_MA_BANK0	AA27	MA_BANK(0)	MA_DATA(39)
12,13 MEM_MA_CKE1	>>	MEM_MA_CKE1	L27	MA_CKE(1)	MA_DATA(38)
11,13 MEM_MA_CKE0	>>	MEM_MA_CKE0	M25	MA_CKE(0)	MA_DATA(37)
MEM_MA_ADD15	>>	MEM_MA_ADD15	M27	MA_ADD(15)	MA_DATA(36)
MEM_MA_ADD14	>>	MEM_MA_ADD14	N24	MA_ADD(14)	MA_DATA(35)
MEM_MA_ADD13	>>	MEM_MA_ADD13	AC26	MA_ADD(13)	MA_DATA(34)
MEM_MA_ADD12	>>	MEM_MA_ADD12	N26	MA_ADD(12)	MA_DATA(33)
MEM_MA_ADD11	>>	MEM_MA_ADD11	P25	MA_ADD(11)	MA_DATA(32)
MEM_MA_ADD10	>>	MEM_MA_ADD10	Y25	MA_ADD(10)	MA_DATA(31)
MEM_MA_ADD9	>>	MEM_MA_ADD9	N27	MA_ADD(9)	MA_DATA(30)
MEM_MA_ADD8	>>	MEM_MA_ADD8	R24	MA_ADD(8)	MA_DATA(29)
MEM_MA_ADD7	>>	MEM_MA_ADD7	P27	MA_ADD(7)	MA_DATA(28)
MEM_MA_ADD6	>>	MEM_MA_ADD6	R25	MA_ADD(6)	MA_DATA(27)
MEM_MA_ADD5	>>	MEM_MA_ADD5	R26	MA_ADD(5)	MA_DATA(26)
MEM_MA_ADD4	>>	MEM_MA_ADD4	R27	MA_ADD(4)	MA_DATA(25)
MEM_MA_ADD3	>>	MEM_MA_ADD3	T25	MA_ADD(3)	MA_DATA(24)
MEM_MA_ADD2	>>	MEM_MA_ADD2	U25	MA_ADD(2)	MA_DATA(23)
MEM_MA_ADD1	>>	MEM_MA_ADD1	T27	MA_ADD(1)	MA_DATA(22)
MEM_MA_ADD0	>>	MEM_MA_ADD0	W24	MA_ADD(0)	MA_DATA(21)
MEM_MA_DQS_H7	>>	MEM_MA_DQS_H7	AD15	MA_DQS_H(7)	MA_DATA(20)
MEM_MA_DQS_L7	>>	MEM_MA_DQS_L7	AE15	MA_DQS_L(7)	MA_DATA(19)
MEM_MA_DQS_H6	>>	MEM_MA_DQS_H6	AG18	MA_DQS_H(6)	MA_DATA(18)
MEM_MA_DQS_L6	>>	MEM_MA_DQS_L6	AG19	MA_DQS_L(6)	MA_DATA(17)
MEM_MA_DQS_H5	>>	MEM_MA_DQS_H5	AG24	MA_DQS_H(5)	MA_DATA(16)
MEM_MA_DQS_L5	>>	MEM_MA_DQS_L5	AG25	MA_DQS_L(5)	MA_DATA(15)
MEM_MA_DQS_H4	>>	MEM_MA_DQS_H4	AG27	MA_DQS_H(4)	MA_DATA(14)
MEM_MA_DQS_L4	>>	MEM_MA_DQS_L4	AG28	MA_DQS_L(4)	MA_DATA(13)
MEM_MA_DQS_H3	>>	MEM_MA_DQS_H3	D29	MA_DQS_H(3)	MA_DATA(12)
MEM_MA_DQS_L3	>>	MEM_MA_DQS_L3	C29	MA_DQS_L(3)	MA_DATA(11)
MEM_MA_DQS_H2	>>	MEM_MA_DQS_H2	D25	MA_DQS_H(2)	MA_DATA(10)
MEM_MA_DQS_L2	>>	MEM_MA_DQS_L2	C25	MA_DQS_L(2)	MA_DATA(9)
MEM_MA_DQS_H1	>>	MEM_MA_DQS_H1	E19	MA_DQS_H(1)	MA_DATA(8)
MEM_MA_DQS_L1	>>	MEM_MA_DQS_L1	F19	MA_DQS_L(1)	MA_DATA(7)
MEM_MA_DQS_H0	>>	MEM_MA_DQS_H0	F15	MA_DQS_H(0)	MA_DATA(6)
MEM_MA_DQS_L0	>>	MEM_MA_DQS_L0	G15	MA_DQS_L(0)	MA_DATA(5)
MEM_MA_DM7	>>	MEM_MA_DM7	AE15	MA_DM(7)	MA_DATA(4)
MEM_MA_DM6	>>	MEM_MA_DM6	AE19	MA_DM(6)	MA_DATA(3)
MEM_MA_DM5	>>	MEM_MA_DM5	AJ25	MA_DM(5)	MA_DATA(2)
MEM_MA_DM4	>>	MEM_MA_DM4	AH29	MA_DM(4)	MA_DATA(1)
MEM_MA_DM3	>>	MEM_MA_DM3	B29	MA_DM(3)	MA_DATA(0)
MEM_MA_DM2	>>	MEM_MA_DM2	E24	MA_DM(2)	
MEM_MA_DM1	>>	MEM_MA_DM1	E18	MA_DM(1)	
MEM_MA_DM0	>>	MEM_MA_DM0	H15	MA_DM(0)	

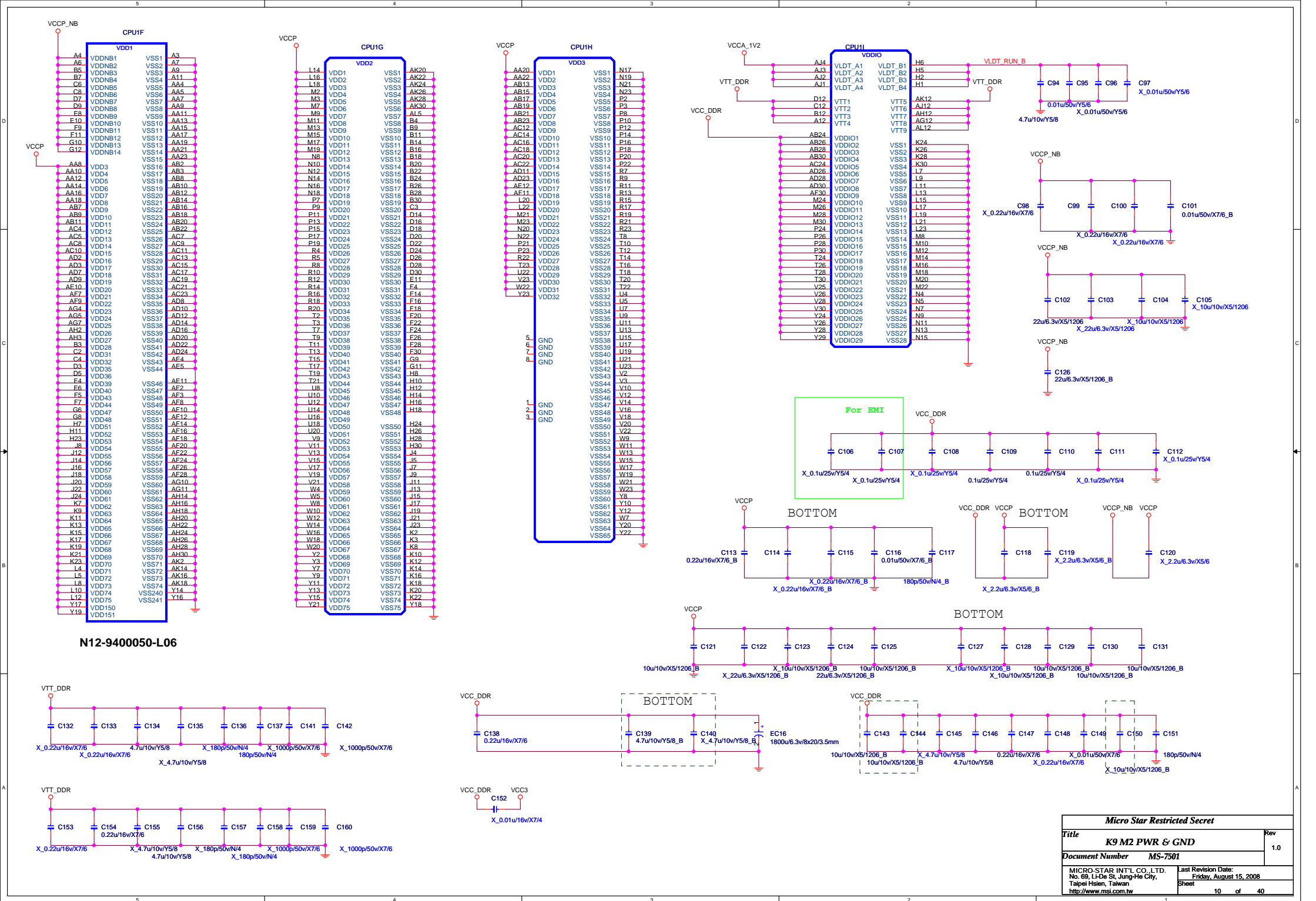
CPU1C

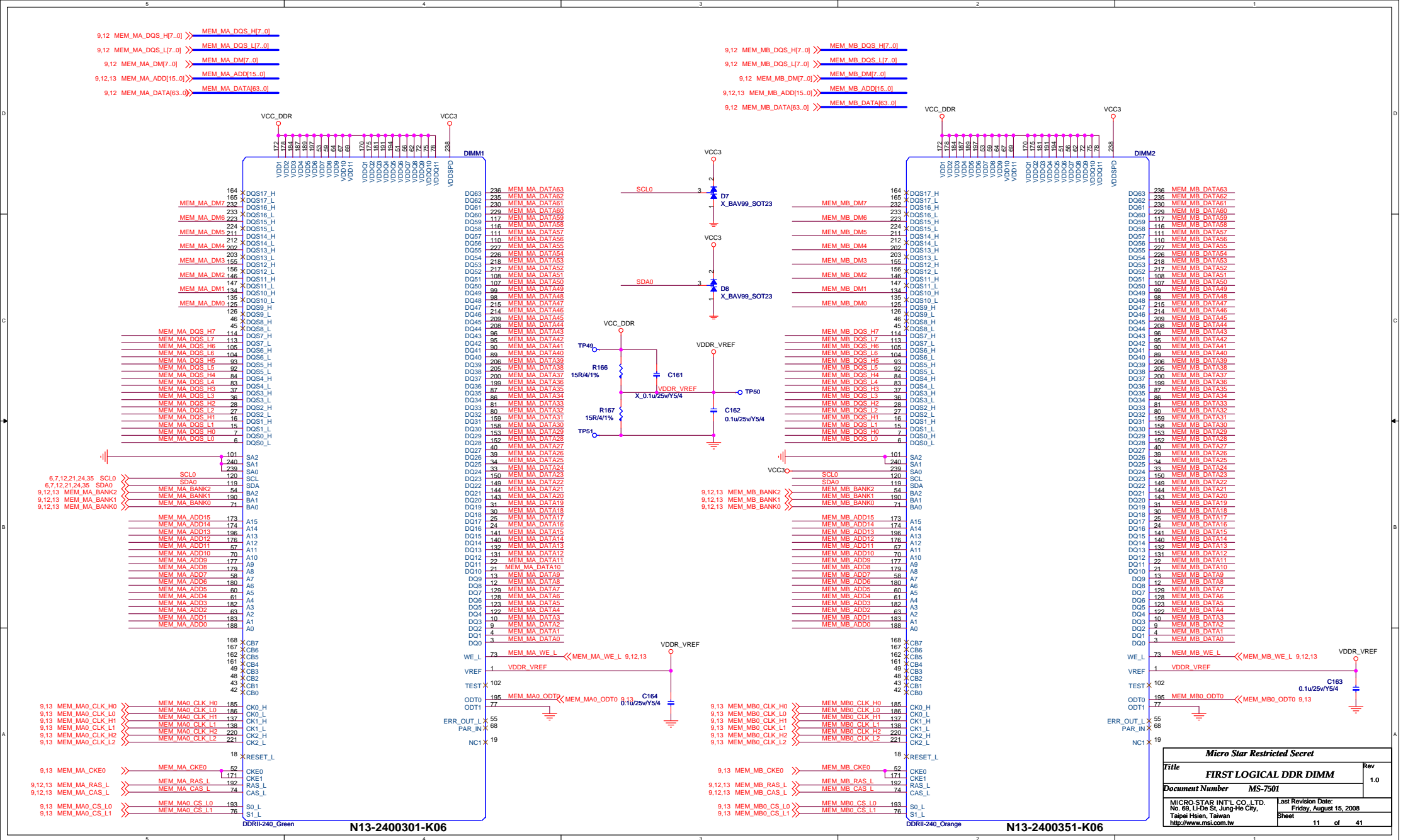
MEMORY INTERFACE B

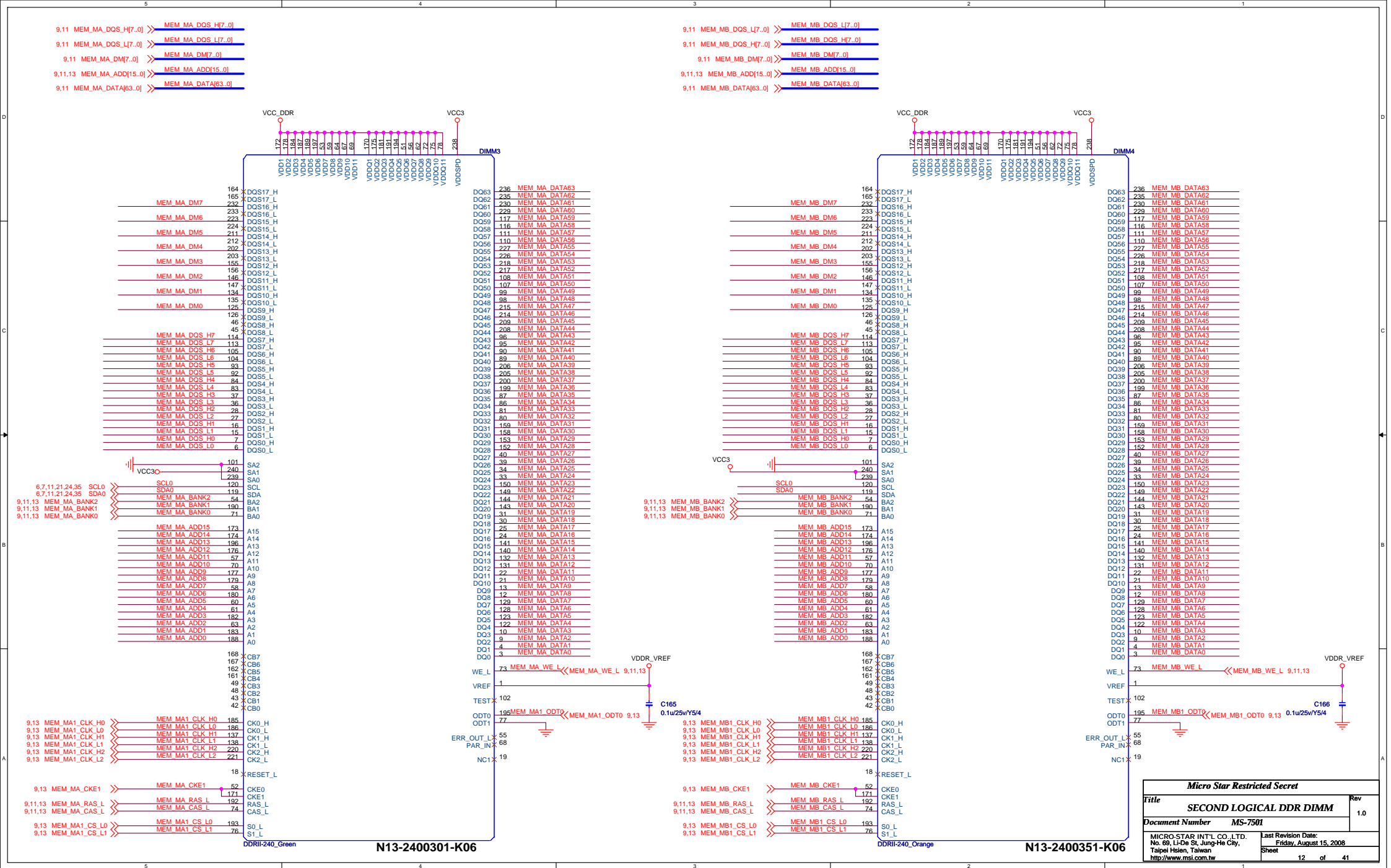
11,13 MEM_MB0_CLK_H2	>>	MEM_MB0_CLK_H2	AJ19	MB0_CLK_H(2)	MB_DATA(63)
11,13 MEM_MB0_CLK_L2	>>	MEM_MB0_CLK_L2	AK19	MB0_CLK_L(2)	MB_DATA(62)
11,13 MEM_MB0_CLK_H1	>>	MEM_MB0_CLK_H1	A18	MB0_CLK_H(1)	MB_DATA(61)
11,13 MEM_MB0_CLK_L1	>>	MEM_MB0_CLK_L1	A19	MB0_CLK_L(1)	MB_DATA(60)
11,13 MEM_MB0_CLK_H0	>>	MEM_MB0_CLK_H0	U31	MB0_CLK_H(0)	MB_DATA(59)
11,13 MEM_MB0_CLK_L0	>>	MEM_MB0_CLK_L0	U30	MB0_CLK_L(0)	MB_DATA(58)
11,13 MEM_MB0_CS_L1	>>	MEM_MB0_CS_L1	AE30	MB0_CS_L(1)	MB_DATA(57)
11,13 MEM_MB0_CS_L0	>>	MEM_MB0_CS_L0	AC31	MB0_CS_L(0)	MB_DATA(56)
11,13 MEM_MB0_ODT0	>>	MEM_MB0_ODT0	AD29	MB0_ODT(0)	MB_DATA(55)
12,13 MEM_MB1_CLK_H2	>>	MEM_MB1_CLK_H2	AL19	MB1_CLK_H(2)	MB_DATA(54)
12,13 MEM_MB1_CLK_L2	>>	MEM_MB1_CLK_L2	AL18	MB1_CLK_L(2)	MB_DATA(53)
12,13 MEM_MB1_CLK_H1	>>	MEM_MB1_CLK_H1	C18	MB1_CLK_H(1)	MB_DATA(52)
12,13 MEM_MB1_CLK_L1	>>	MEM_MB1_CLK_L1	D19	MB1_CLK_L(1)	MB_DATA(51)
12,13 MEM_MB1_CLK_H0	>>	MEM_MB1_CLK_H0	W29	MB1_CLK_H(0)	MB_DATA(50)
12,13 MEM_MB1_CLK_L0	>>	MEM_MB1_CLK_L0	W28	MB1_CLK_L(0)	MB_DATA(49)
12,13 MEM_MB1_CS_L1	>>	MEM_MB1_CS_L1	AE29	MB1_CS_L(1)	MB_DATA(48)
12,13 MEM_MB1_CS_L0	>>	MEM_MB1_CS_L0	AB31	MB1_CS_L(0)	MB_DATA(47)
12,13 MEM_MB1_ODT0	>>	MEM_MB1_ODT0	AD31	MB1_ODT(0)	MB_DATA(46)
11,12,13 MEM_MB_CAS_L	>>	MEM_MB_CAS_L	AC29	MB_CAS_L	MB_DATA(45)
11,12,13 MEM_MB_WE_L	>>	MEM_MB_WE_L	AC30	MB_WE_L	MB_DATA(44)
11,12,13 MEM_MB_RAS_L	>>	MEM_MB_RAS_L	AB29	MB_RAS_L	MB_DATA(43)
11,12,13 MEM_MB_BANK2	>>	MEM_MB_BANK2	N31	MB_BANK(2)	MB_DATA(42)
11,12,13 MEM_MB_BANK1	>>	MEM_MB_BANK1	AA31	MB_BANK(1)	MB_DATA(41)
11,12,13 MEM_MB_BANK0	>>	MEM_MB_BANK0	AA28	MB_BANK(0)	MB_DATA(40)
12,13 MEM_MB_CKE1	>>	MEM_MB_CKE1	M31	MB_CKE(1)	MB_DATA(39)
11,13 MEM_MB_CKE0	>>	MEM_MB_CKE0	M29	MB_CKE(0)	MB_DATA(38)
MEM_MB_ADD15	>>	MEM_MB_ADD15	N28	MB_ADD(15)	MB_DATA(37)
MEM_MB_ADD14	>>	MEM_MB_ADD14	N29	MB_ADD(14)	MB_DATA(36)
MEM_MB_ADD13	>>	MEM_MB_ADD13	AE31	MB_ADD(13)	MB_DATA(35)
MEM_MB_ADD12	>>	MEM_MB_ADD12	N30	MB_ADD(12)	MB_DATA(34)
MEM_MB_ADD11	>>	MEM_MB_ADD11	P29	MB_ADD(11)	MB_DATA(33)
MEM_MB_ADD10	>>	MEM_MB_ADD10	AA29	MB_ADD(10)	MB_DATA(32)
MEM_MB_ADD9	>>	MEM_MB_ADD9	P31	MB_ADD(9)	MB_DATA(31)
MEM_MB_ADD8	>>	MEM_MB_ADD8	R29	MB_ADD(8)	MB_DATA(30)
MEM_MB_ADD7	>>	MEM_MB_ADD7	R28	MB_ADD(7)	MB_DATA(29)
MEM_MB_ADD6	>>	MEM_MB_ADD6	R31	MB_ADD(6)	MB_DATA(28)
MEM_MB_ADD5	>>	MEM_MB_ADD5	R30	MB_ADD(5)	MB_DATA(27)
MEM_MB_ADD4	>>	MEM_MB_ADD4	T31	MB_ADD(4)	MB_DATA(26)
MEM_MB_ADD3	>>	MEM_MB_ADD3	T29	MB_ADD(3)	MB_DATA(25)
MEM_MB_ADD2	>>	MEM_MB_ADD2	U29	MB_ADD(2)	MB_DATA(24)
MEM_MB_ADD1	>>	MEM_MB_ADD1	U28	MB_ADD(1)	MB_DATA(23)
MEM_MB_ADD0	>>	MEM_MB_ADD0	AA30	MB_ADD(0)	MB_DATA(22)
MEM_MB_DQS_H7	>>	MEM_MB_DQS_H7	AK13	MB_DQS_H(7)	MB_DATA(21)
MEM_MB_DQS_L7	>>	MEM_MB_DQS_L7	AJ13	MB_DQS_L(7)	MB_DATA(20)
MEM_MB_DQS_H6	>>	MEM_MB_DQS_H6	AK17	MB_DQS_H(6)	MB_DATA(19)
MEM_MB_DQS_L6	>>	MEM_MB_DQS_L6	AJ17	MB_DQS_L(6)	MB_DATA(18)
MEM_MB_DQS_H5	>>	MEM_MB_DQS_H5	AK23	MB_DQS_H(5)	MB_DATA(17)
MEM_MB_DQS_L5	>>	MEM_MB_DQS_L5	AL23	MB_DQS_L(5)	MB_DATA(16)
MEM_MB_DQS_H4	>>	MEM_MB_DQS_H4	AL28	MB_DQS_H(4)	MB_DATA(15)
MEM_MB_DQS_L4	>>	MEM_MB_DQS_L4	AL29	MB_DQS_L(4)	MB_DATA(14)
MEM_MB_DQS_H3	>>	MEM_MB_DQS_H3	D31	MB_DQS_H(3)	MB_DATA(13)
MEM_MB_DQS_L3	>>	MEM_MB_DQS_L3	C31	MB_DQS_L(3)	MB_DATA(12)
MEM_MB_DQS_H2	>>	MEM_MB_DQS_H2	C24	MB_DQS_H(2)	MB_DATA(11)
MEM_MB_DQS_L2	>>	MEM_MB_DQS_L2	C24	MB_DQS_L(2)	MB_DATA(10)
MEM_MB_DQS_H1	>>	MEM_MB_DQS_H1	D17	MB_DQS_H(1)	MB_DATA(9)
MEM_MB_DQS_L1	>>	MEM_MB_DQS_L1	C17	MB_DQS_L(1)	MB_DATA(8)
MEM_MB_DQS_H0	>>	MEM_MB_DQS_H0	C14	MB_DQS_H(0)	MB_DATA(7)
MEM_MB_DQS_L0	>>	MEM_MB_DQS_L0	C13	MB_DQS_L(0)	MB_DATA(6)
MEM_MB_DM7	>>	MEM_MB_DM7	AJ14	MB_DM(7)	MB_DATA(5)
MEM_MB_DM6	>>	MEM_MB_DM6	AH17	MB_DM(6)	MB_DATA(4)
MEM_MB_DM5	>>	MEM_MB_DM5	AJ23	MB_DM(5)	MB_DATA(3)
MEM_MB_DM4	>>	MEM_MB_DM4	AK29	MB_DM(4)	MB_DATA(2)
MEM_MB_DM3	>>	MEM_MB_DM3	C30	MB_DM(3)	MB_DATA(1)
MEM_MB_DM2	>>	MEM_MB_DM2	A27	MB_DM(2)	MB_DATA(0)
MEM_MB_DM1	>>	MEM_MB_DM1	B17	MB_DM(1)	
MEM_MB_DM0	>>	MEM_MB_DM0	B13	MB_DM(0)	

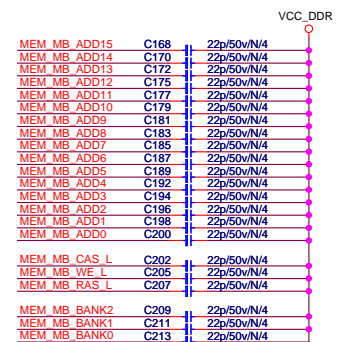
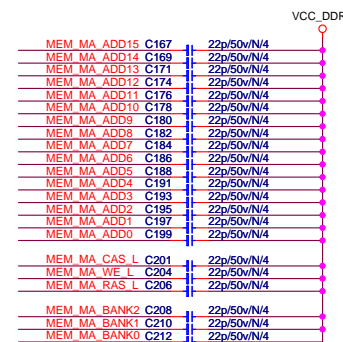
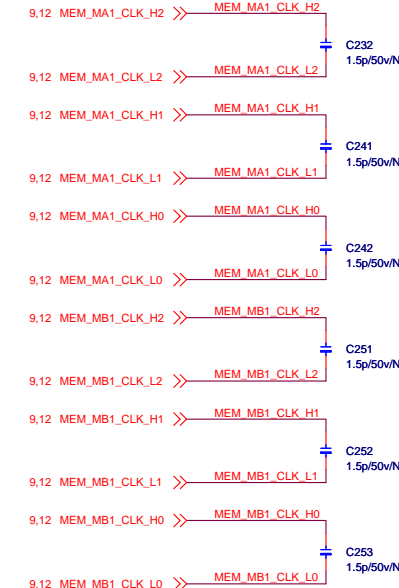
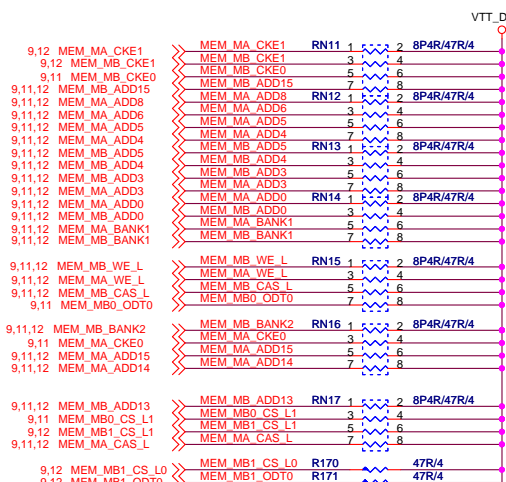
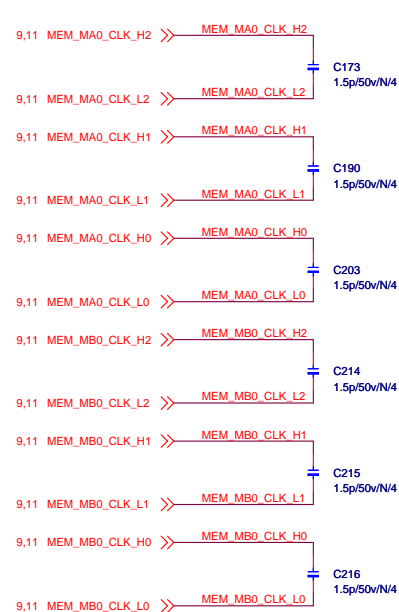
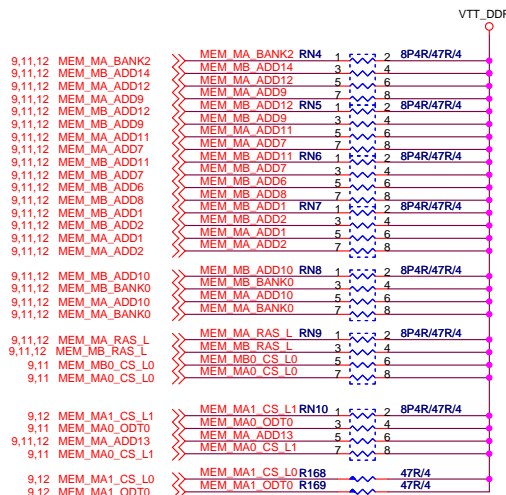
Micro Star Restricted Secret

Title	K9 M2 DDR MEMORY I/F	Rev	1.0
Document Number	MS-7501		
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>		Last Revision Date: Friday, August 15, 2008 Sheet	
		9	of 41

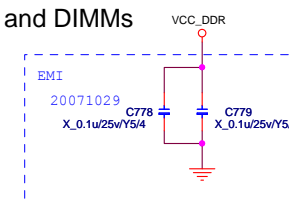




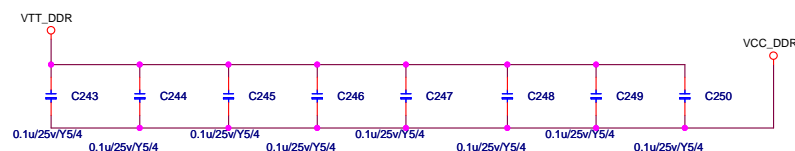
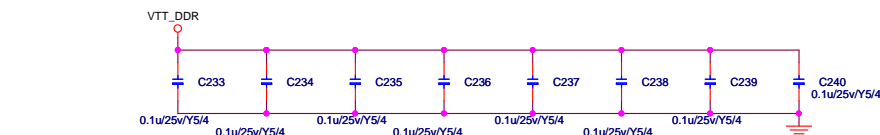
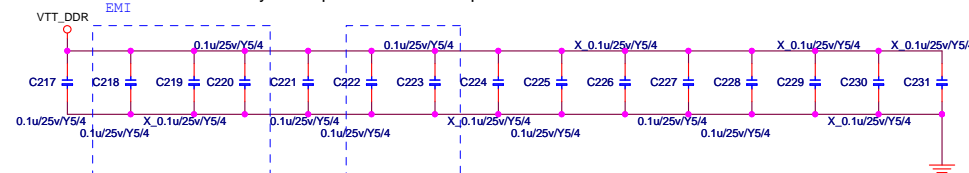




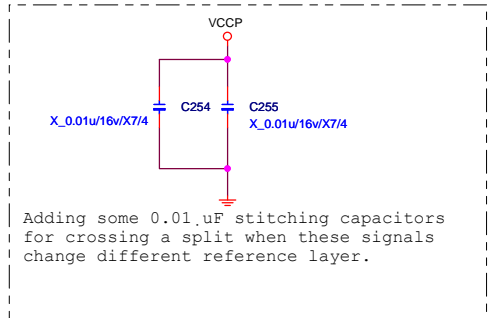
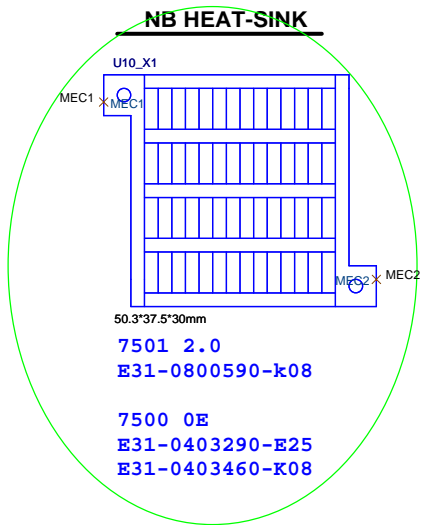
## Decoupling Between Processor and DIMMs



Layout: Spread out on VTT pour



Micro Star Restricted Secret		
Title	DDR Termination	Rev 1.0
Document Number	MS-7501	
MICRO-STAR INT'L CO., LTD. No. 69, Li-Ho St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, August 15, 2008 Sheet 13 of 40

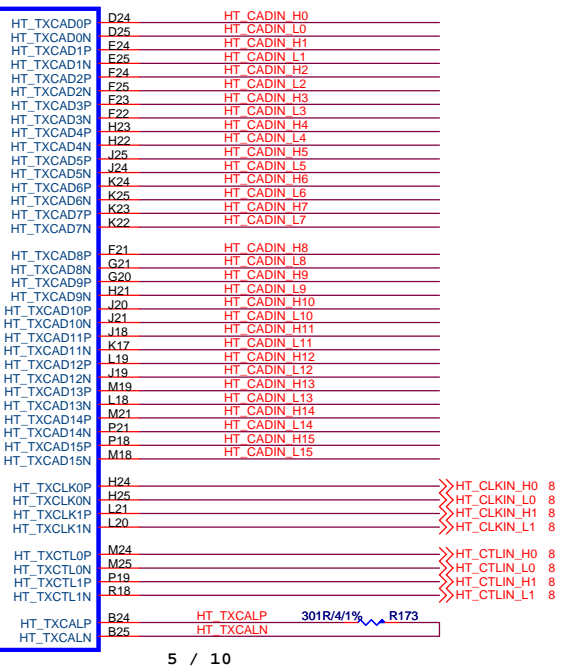
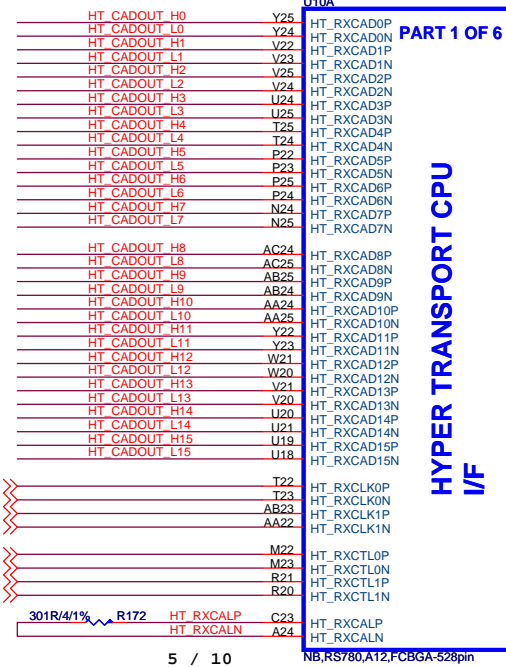


8 HT\_CADOUT\_H[15..0] >> HT\_CADOUT\_H[15..0]  
8 HT\_CADOUT\_L[15..0] >> HT\_CADOUT\_L[15..0]

8 HT\_CADIN\_H[15..0] >> HT\_CADIN\_H[15..0]  
8 HT\_CADIN\_L[15..0] >> HT\_CADIN\_L[15..0]

20 / 5 / 5 / 5 / 20

20 / 5 / 5 / 5 / 20

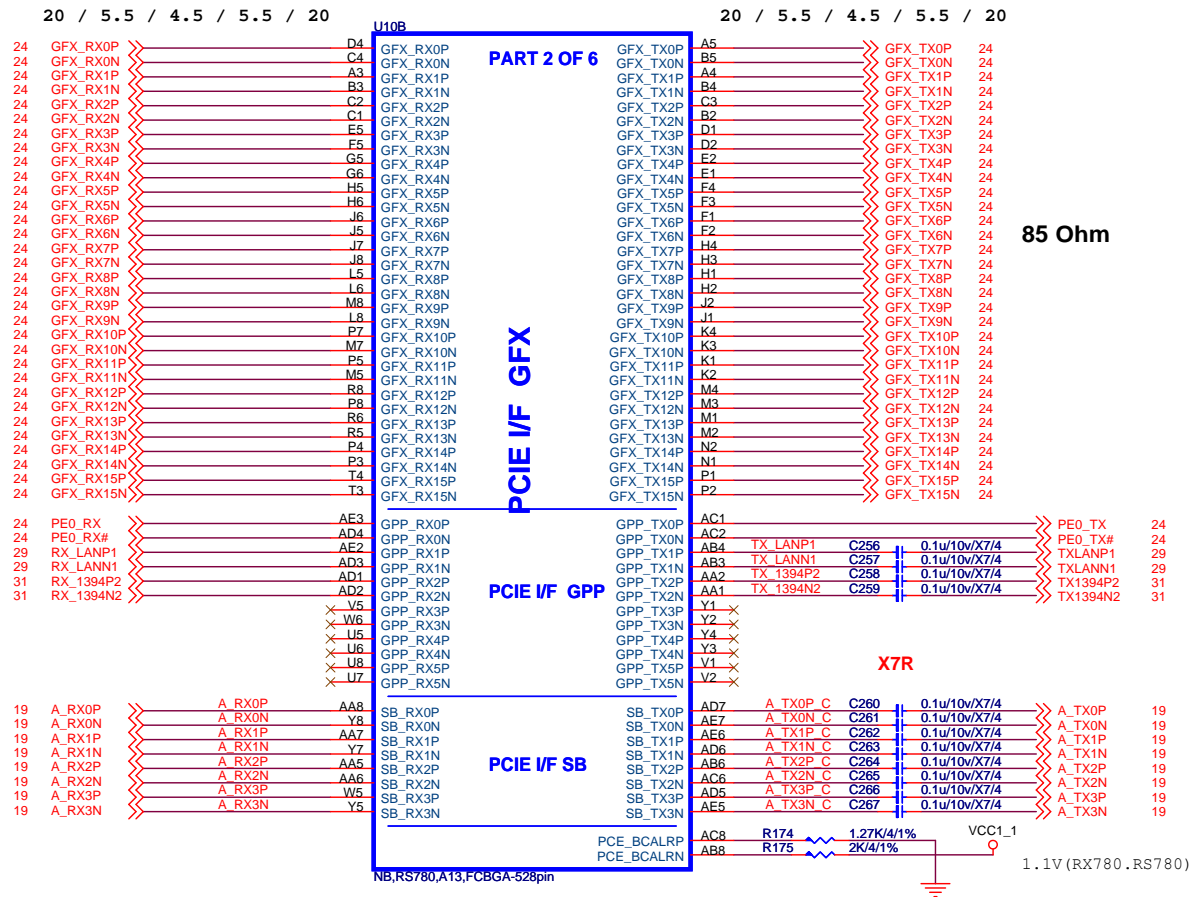


**B01-RS78085-A08**

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)	1.21K	301R
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



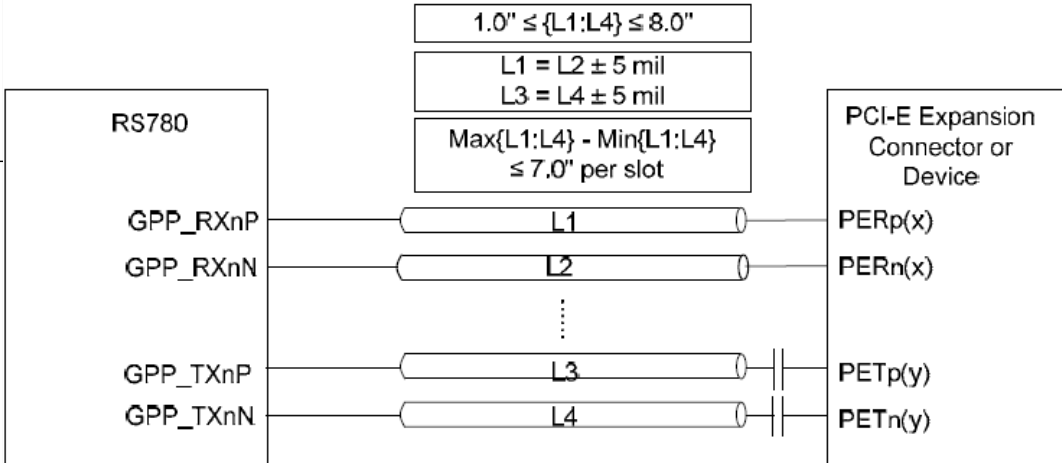


1.0" ≤ {L1:L4} ≤ 8.0"

L1 = L2 ± 5 mil

L3 = L4 ± 5 mil

Max{L1:L4} - Min{L1:L4} ≤ 7.0" per slot



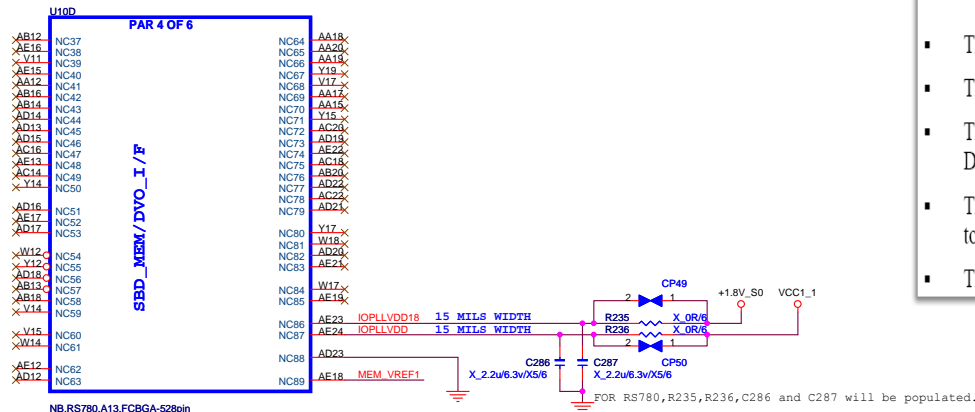
RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Figure 39: Layout Guidelines for the PCI-Express Expansion Interface

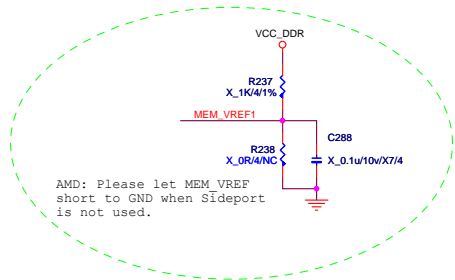






Note: If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD\_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18\_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM\_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT\_GPIO0 is **not** connected to the GND.



## Max Power Estimates for RS780 and SB700

(Preliminary Data w/ Internal Clock Generator and IMC disabled)

April 2007

Voltage	Usage	Domain	Max(Spec)
1.0-1.1V	RS780	S0/S1	10A
1.1V	RS780	S0/S1	3-4A
1.2V	RS780 & SB700	S0/S1	2.4A (1A-NB / 1.4A-SB)
1.8V	RS780& SB700	S0/S1	0.8A (0.75A-NB / 50mA-SB)

## Max Power Estimates for RS780 and SB700 (continued)

April 2007

Voltage	Usage	Domain	Max(Spec)
3.3V	RS780& SB700	S0/S1	428mA (0.3A-NB / 128mA-SB)
1.2VDual	SB700	S0/S1/S2/S3/S4/S5	217mA
3.3VDual	SB700	S0/S1/S2/S3/S4/S5	495mA
5V	SB700 V5_VREF	S0/S1	0.21mA

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Size Document Number MS-7501

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Rev 1.0

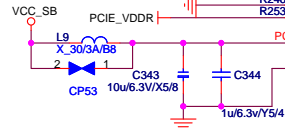


## SB HEAT SINK

U13\_X1

MSI  
DDRE31-0402860-K08 7302  
E31-0402470-K08 7500PLACE PCIE CAPS  
CLOSE TO U13

100 Ohm



100 Ohm

TP26

X\_0R/4\_B

R257

X\_0R/4\_B

R260

X\_20M/6

R266

X\_20M/6

C346

12p/50v/N/6

C347

12p/50v/N/6

PLACE THESE COMPONENTS CLOSE TO U600, AND  
USE GROUND GUARD FOR 32K\_X1 AND 32K\_X2

Note: LDT\_PG, LDT\_STP# & LDT\_RST# are OD  
and require a PU to the CPU I/O rail. They are  
also in the S5 domain to prevent glitching at  
power up.

SB,SB700,A12,FCBGA-528pin

B01-SB70035-A08

SB700  
Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC

CPU

RTC

INTRUDER\_ALERT#

VBAT

RTCCLK

PROCHOT#

LDRQ1#/GNT5#/GPIO68

BMREQ#/REQ5#/GPIO65

SERIRQ

LPCCLK0

LPCCLK1

LAD0

LAD1

LAD2

LAD3

LFRAME#

LDRQ0#

LDRQ1#

LDRQ2#

LDRQ3#

LDRQ4#

LDRQ5#

LDRQ6#

LDRQ7#

LDRQ8#

LDRQ9#

LDRQ10#

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LDRQ271#

LDRQ272#

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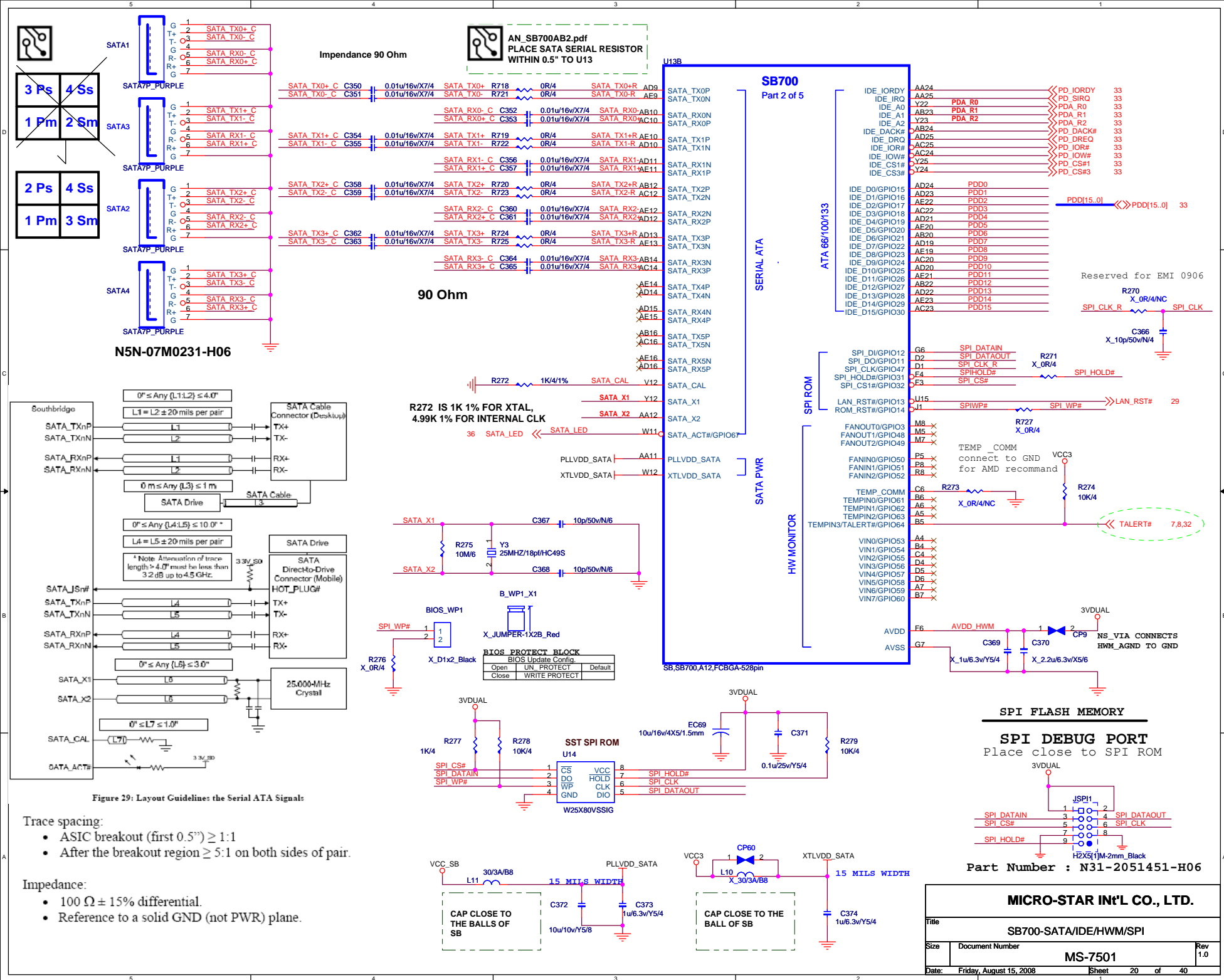
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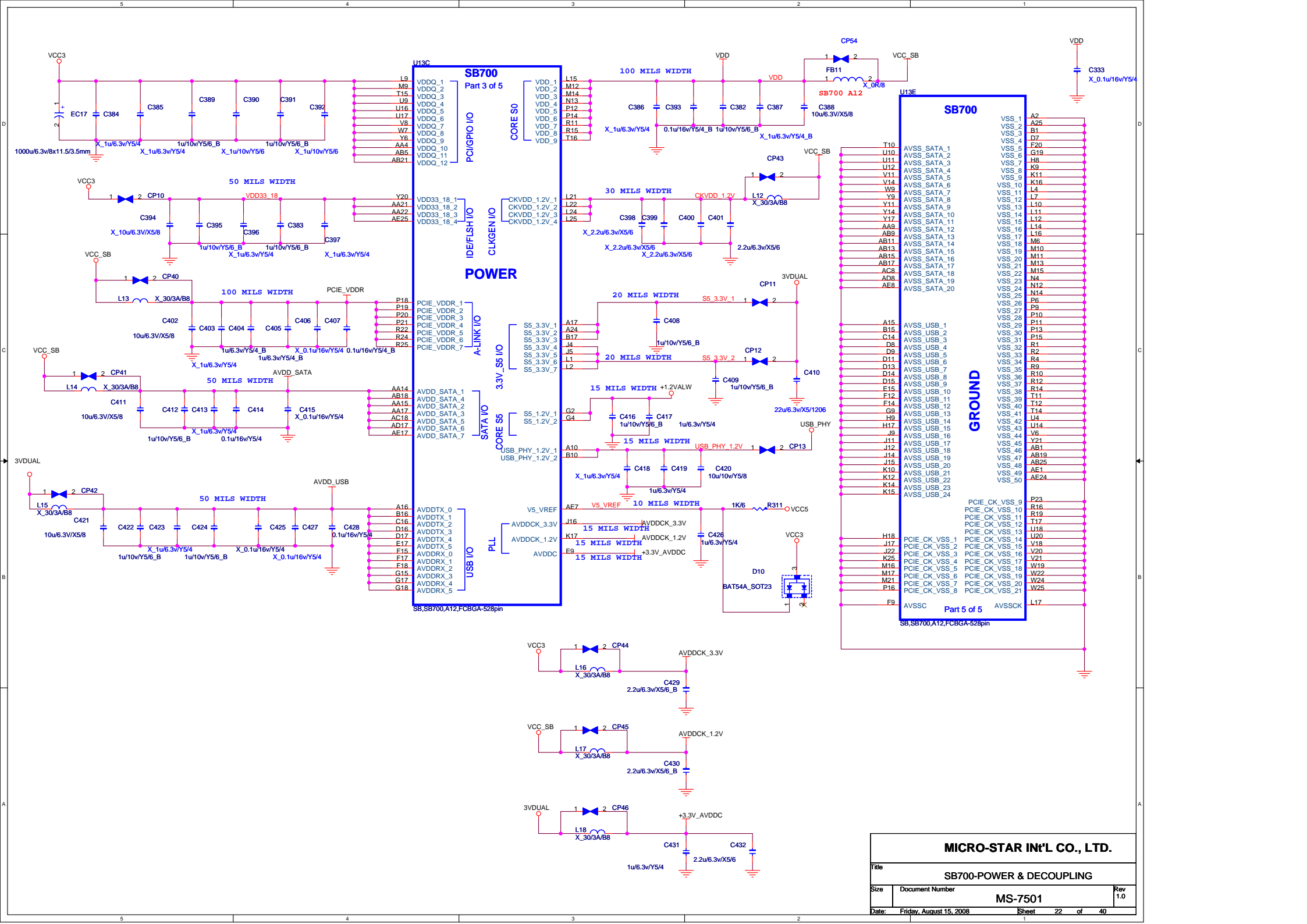
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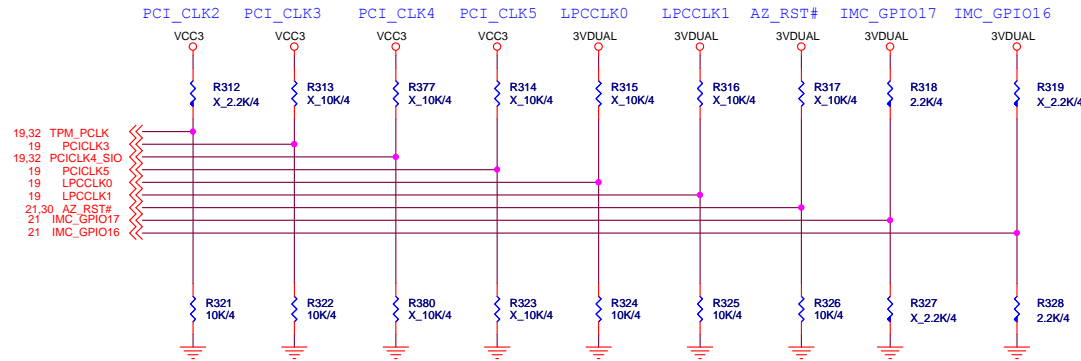






## REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM DEFAULT	

## DEBUG STRAPS

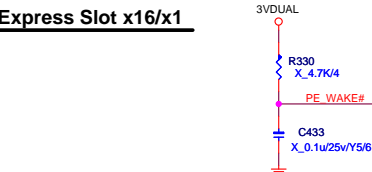
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

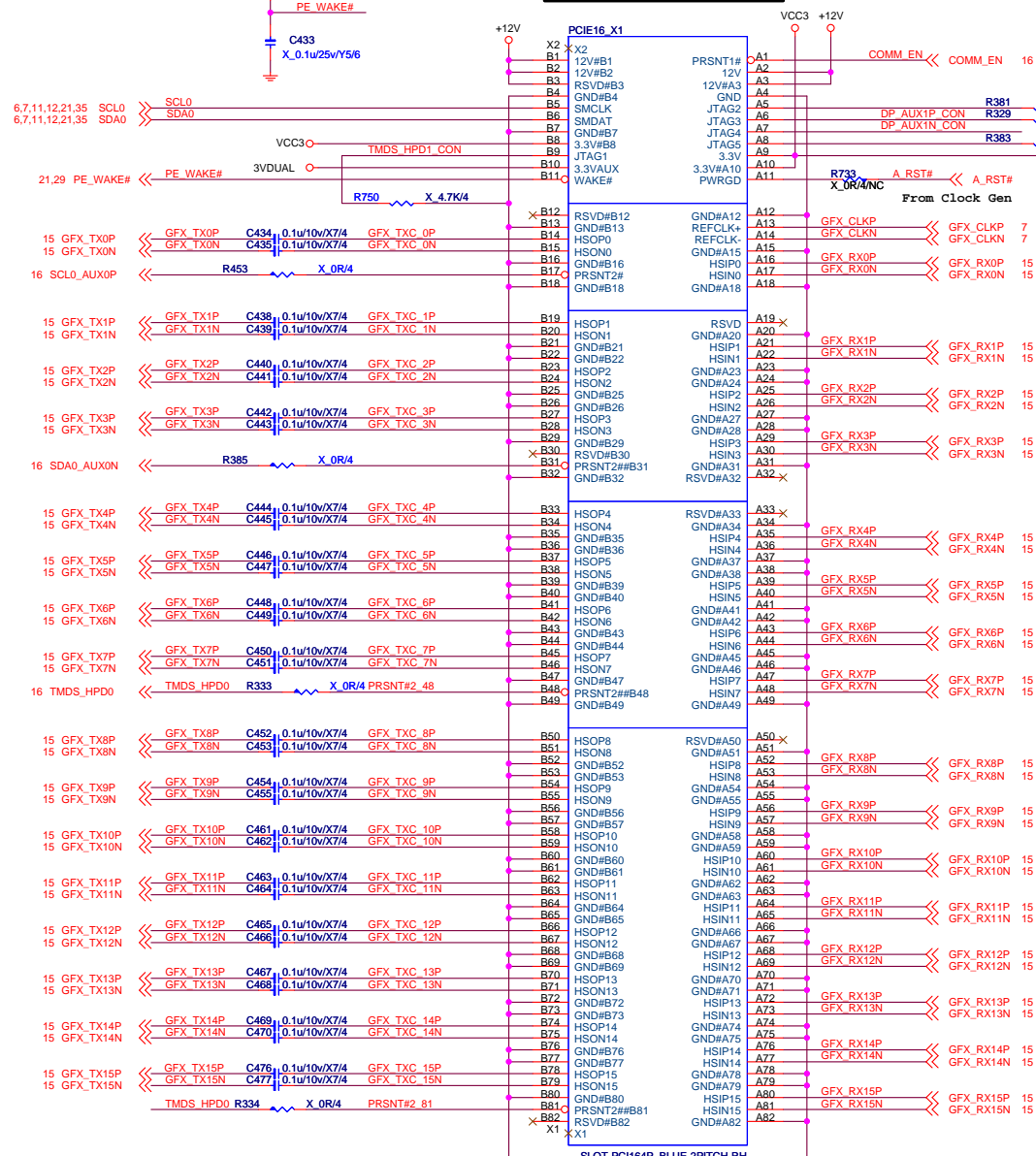
MICRO-STAR INT'L CO., LTD.

Title			
SB700-STRAPS			
Size	Document Number		Rev 1.0
	MS-7501		
Date:	Friday, August 15, 2008		Sheet 23 of 40

# PCI Express Slot x16/x1

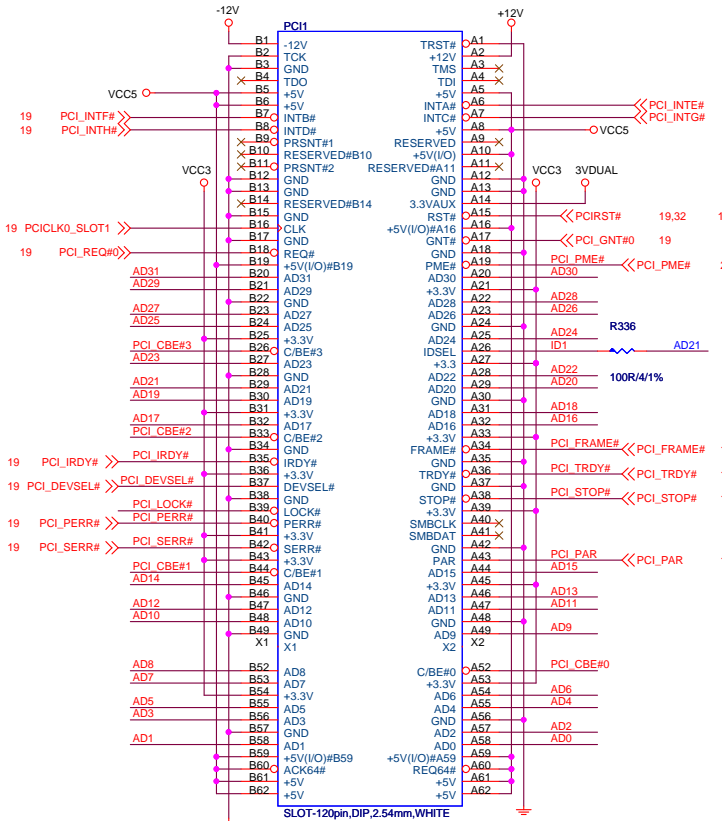


## PCI EXPRESS x16 Slot



19 AD[31..0] >> AD[31..0]  
19 PCI\_CBE#[3..0] >> PCI\_CBE#[3..0]

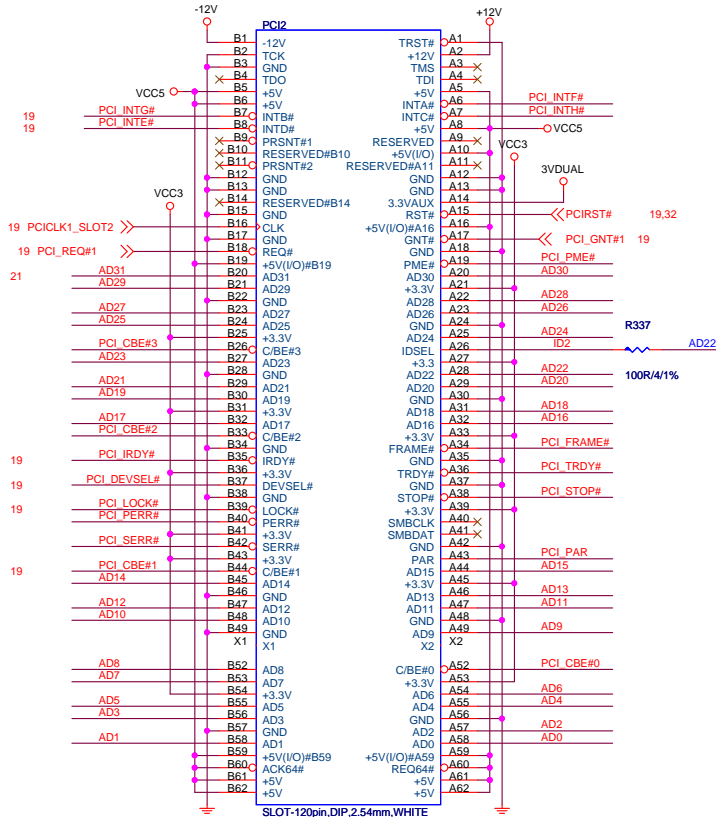
### PCI SLOT 1 (PCI VER: 2.2 COMPLY)



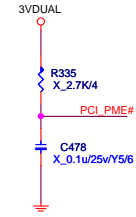
IDSEL = AD21  
MASTER = PCI\_REQ#0  
PCI\_GNT#0

N11-1200271-F02

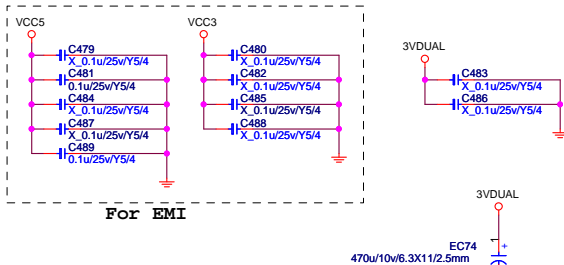
### PCI SLOT 2 (PCI VER: 2.2 COMPLY)



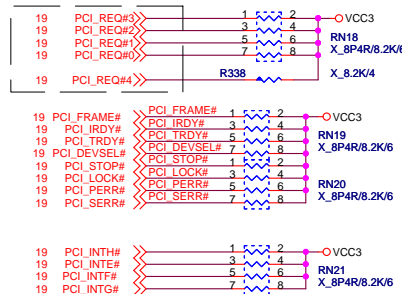
IDSEL = AD22  
MASTER = PCI\_REQ#1  
PCI\_GNT#1



### PCI SLOT DECOUPLING CAPACITORS

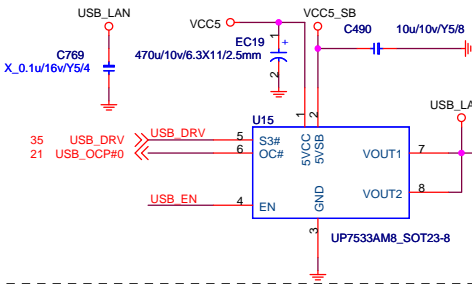


### PCI PULL-UP / DOWN RESISTORS

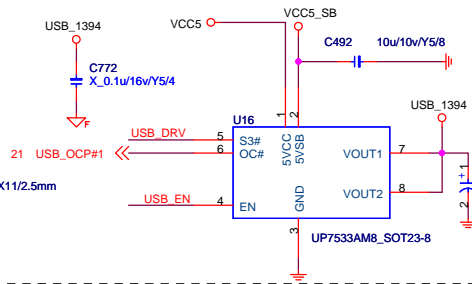


Micro Star Restricted Secret		
Title	PCI Slot 1 2	Rev 1.0
Document Number	MS-7501	
MICRO-STAR INT'L CO., LTD. No. 68, Lihde St, Jung-Ho City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>		
Last Revision Date: Friday, August 15, 2008		
Sheet 25 of 40		

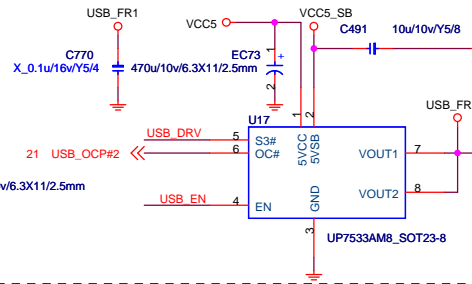
## POWER CIRCUIT FOR USB PORT 4,5



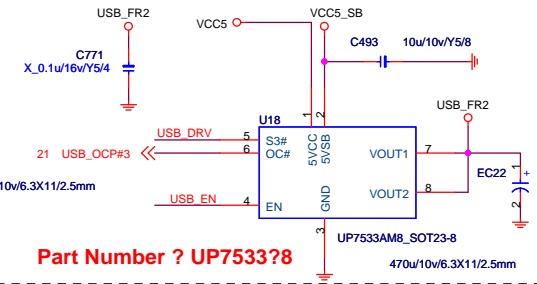
## POWER CIRCUIT FOR USB PORT 2,3



## POWER CIRCUIT FOR USB PORT 0,1



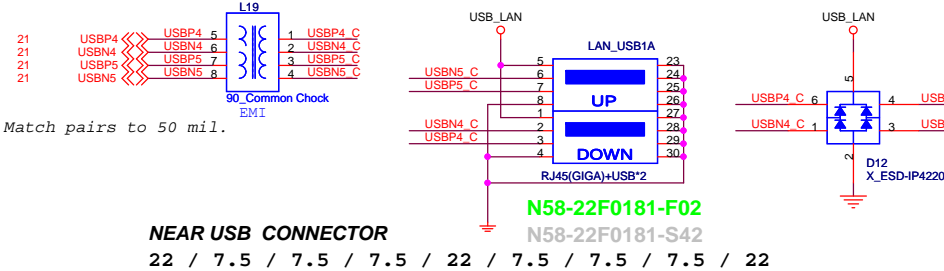
## POWER CIRCUIT FOR USB PORT 6,7



Part Number ? UP7533?8

## REAR PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 12 inches

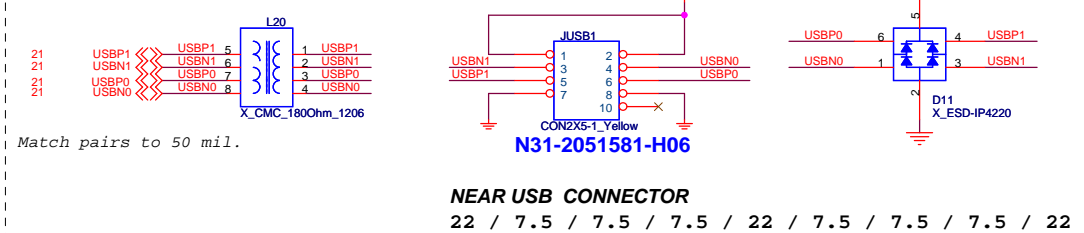


NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

## FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

Trace lengths must be less 5 inches

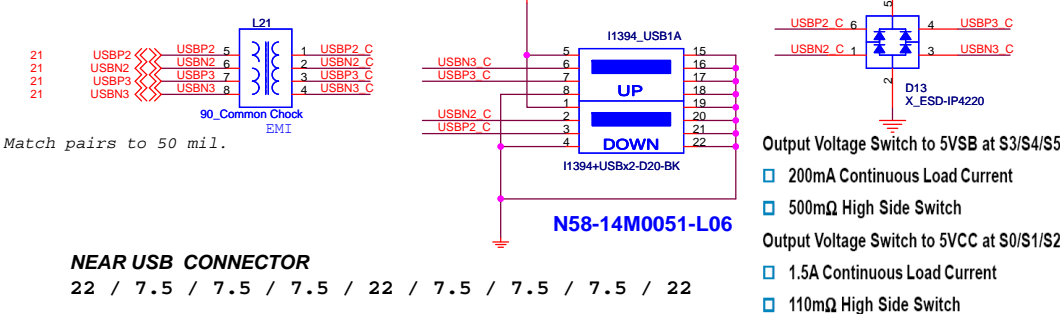


NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

## REAR PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 12 inches

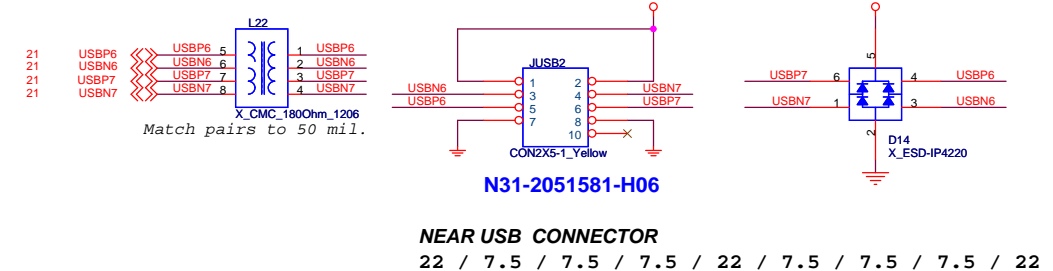


NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches

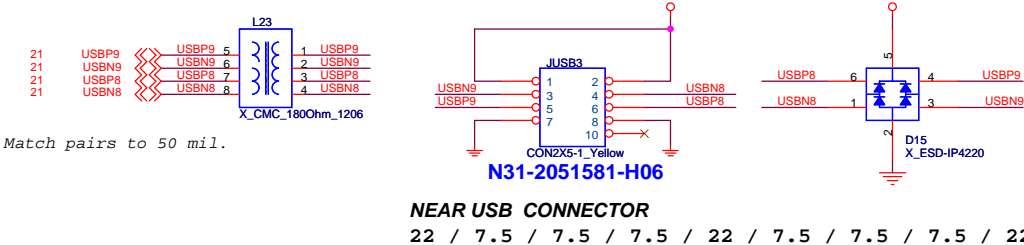


NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

## FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

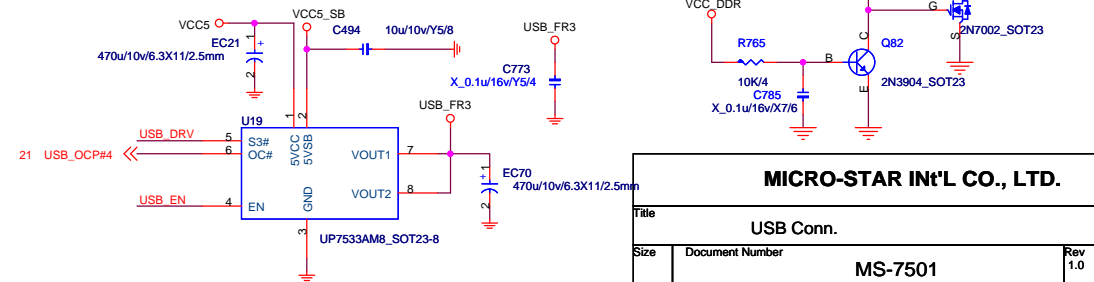
Trace lengths must be less 5 inches



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

## POWER CIRCUIT FOR USB PORT 8,9



MICRO-STAR IN'L CO., LTD.

Title			USB Conn.
Size	Document Number	MS-7501	Rev 1.0
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Place close to VGA/TV connector

100 ohm

100pF

3V

VGA/TV Connector

RS780

RED

RED#

GREEN

GREEN#

BLUE

BLUE#

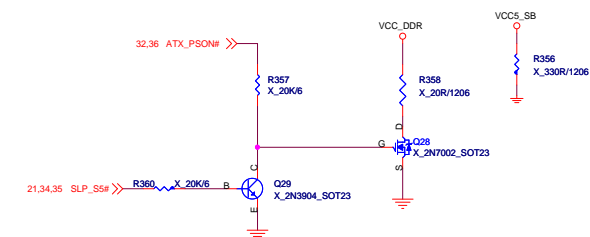
Y

C

COMP

TV Connector

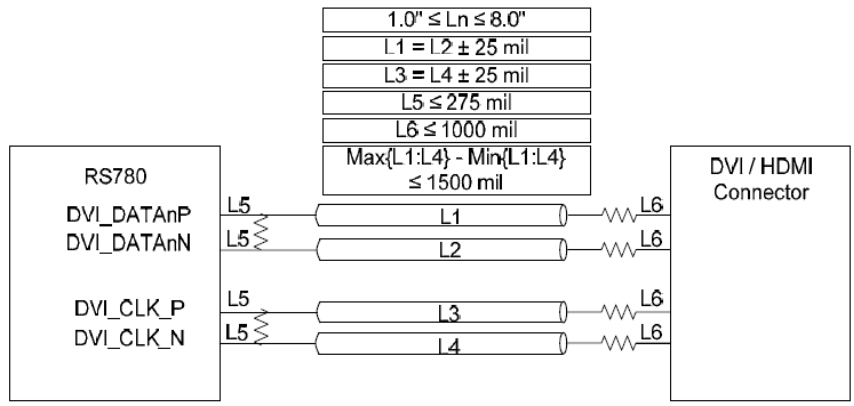
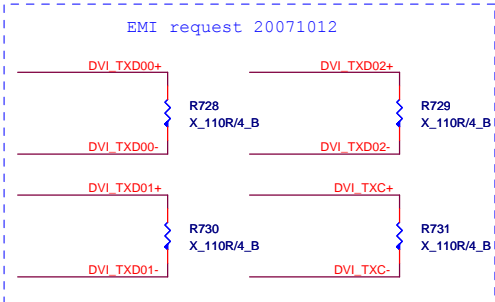
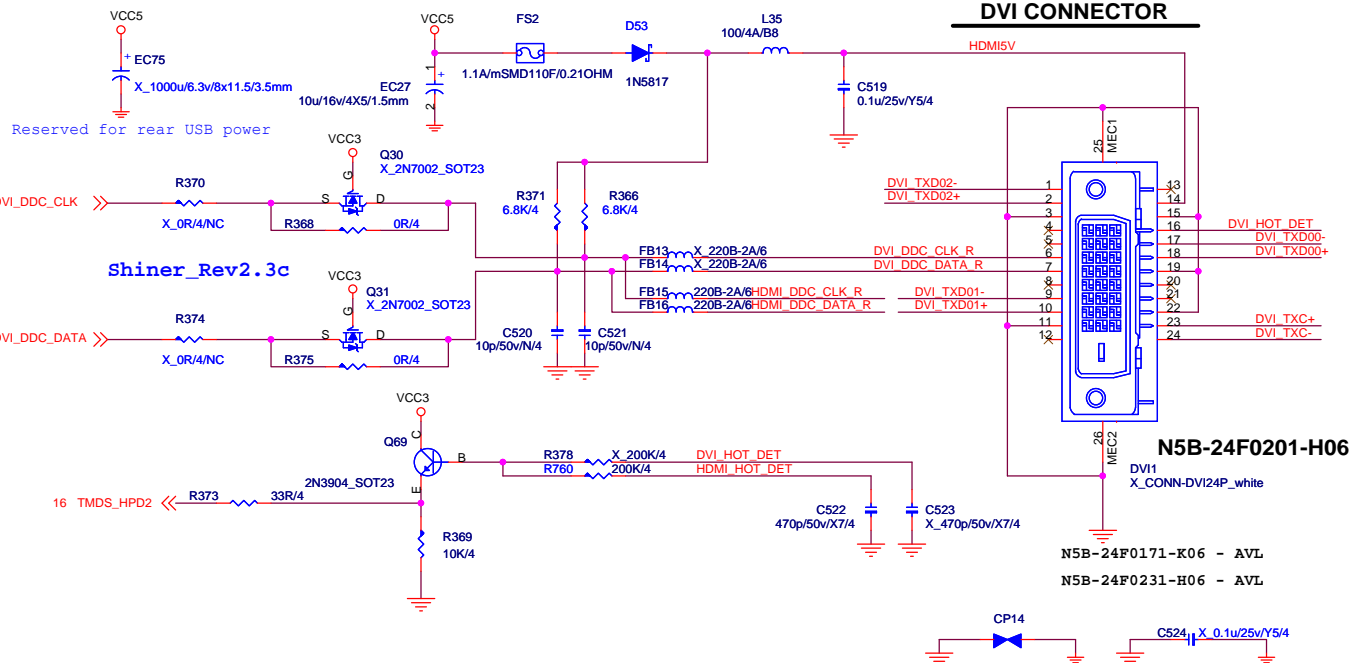
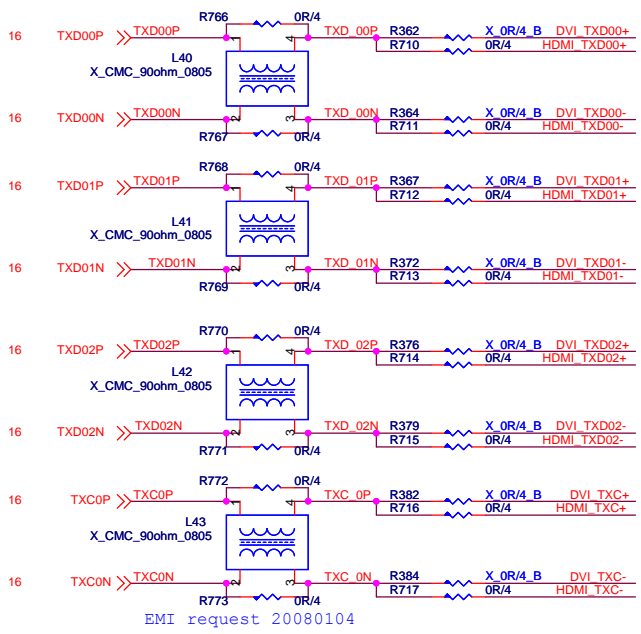
Place close to TV connector



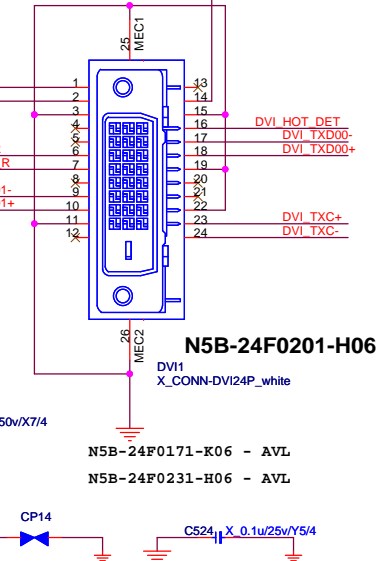
T:2 , H:4.5 ,W:5 ,S:7,Er:4.2 ,Zo=104.8 Ohm

CRB Shiner\_Rev2.1 change to 0 Ohm

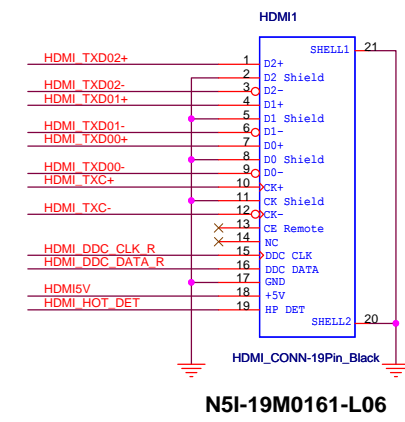
15 / 5 / 7 / 5 / 15



## DVI CONNECTOR



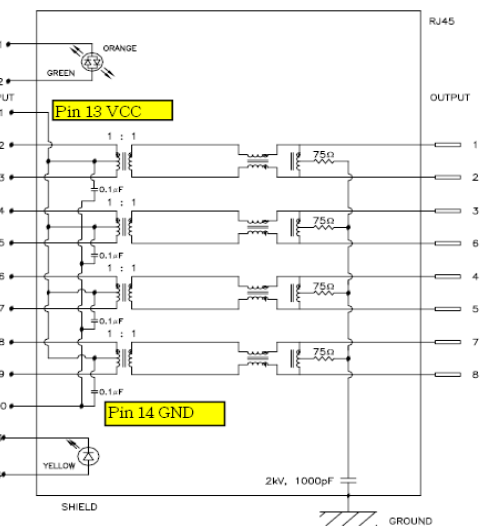
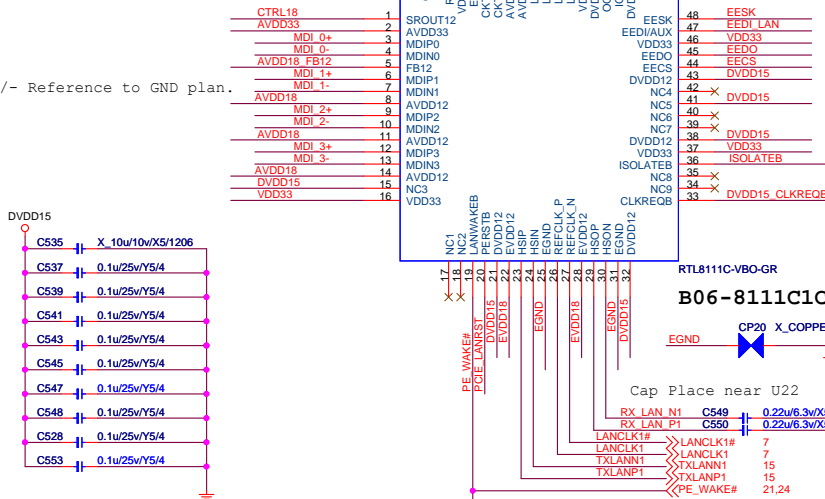
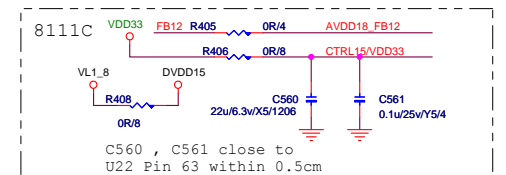
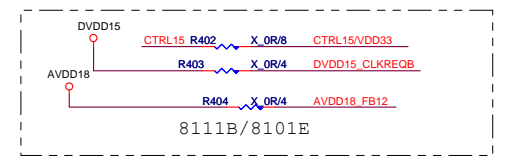
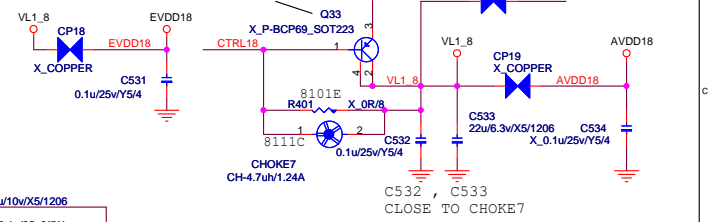
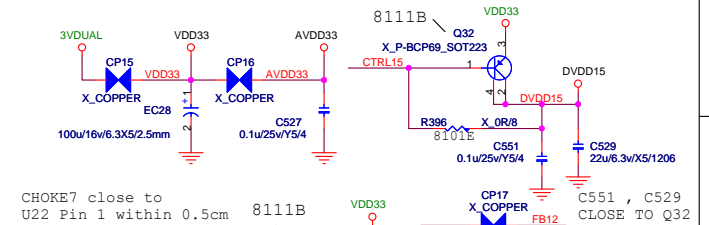
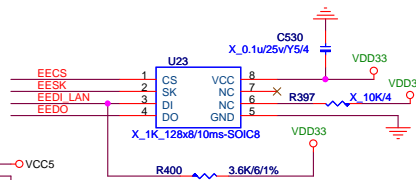
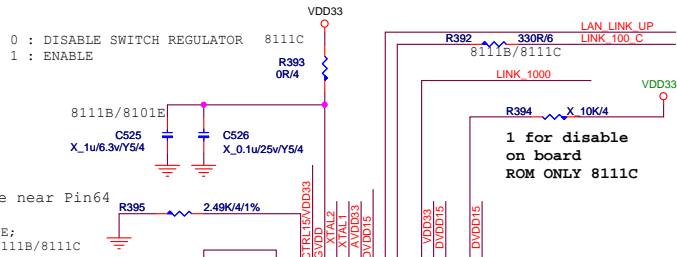
## HDMI CONNECTOR



MICRO-STAR IN'L CO., LTD.			
Title			
HDMI / DVI CONNECTOR			
Size	Document Number	MS-7501	
Date:	Friday, August 15, 2008	Sheet	28 of 41

Figure 32: Layout Guidelines for the DVI/HDMI Signals

- Pin 64:RSET res. should be close to LAN chip. Don't have power trace or high frequency trace beside it.
- The trace of each Pair(MDIX+/-) should be equal in length and better have ground under.
- RTL8111B/C/8101E, Pin 1~16 forward to transformer, this will made the trace more short.
- As the Layout Guide, the output pin of Transistor trace please layout it more widely.
- Make nine through holes at the center of IC board. The back side of IC is GND. Please be aware to connect this GND to the GND of outside of LAN chip.
- Both EGGND and GND can be connect together or use 0 Ohm res. to connect them.
- The Spec of transistor suggest use the current least 1.2A.
- 1.5V請留 power plane並且盡量大一點.
- 1.5V Bypass 電容不能省. Add 0.1u cap. for each power pin of LAN.
- For RTL8111B, Pin62 有外接兩顆電容絕對不能省.

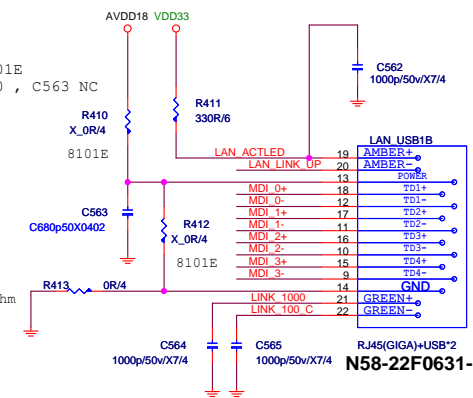


### Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V
RTL8111B	Need	Need
RTL8111C	N/A	N/A
RTL8101E	N/A	N/A

For RTL8101E stuff R410, C563 NC

8111B/8111C to 0 ohm 8101E to 0.01uF



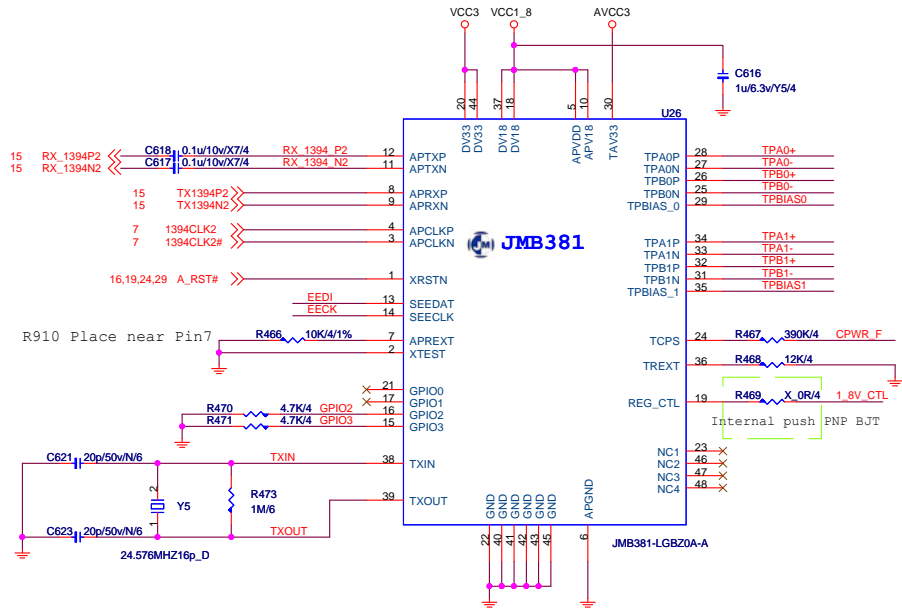
Power consumption		
	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

Giga-Lan		10/100-Lan	
N58-22F0081-S42		N58-22F0061-S42 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19	Yellow	19	Yellow
20	Yellow	20	Yellow
21	Orange	21	Green
22	Green	22	Green

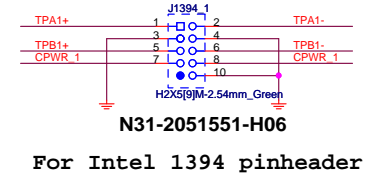
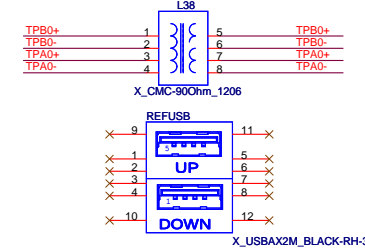
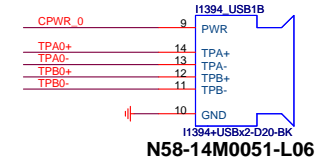
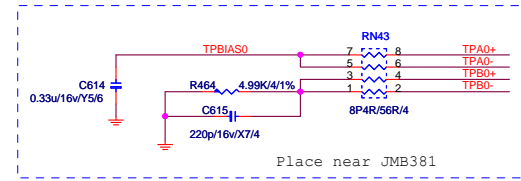




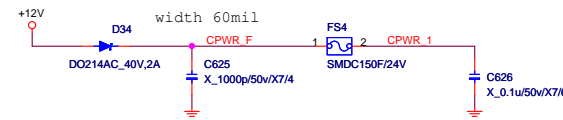
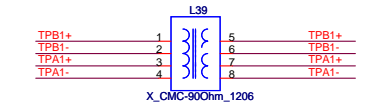
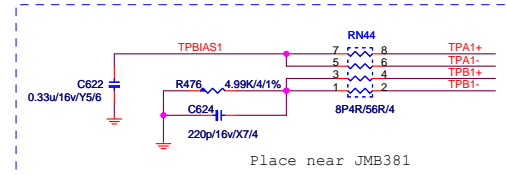
# 1394 CONTROLLER



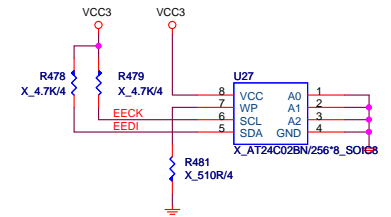
## Rear 1394 port



## Front 1394 pin header



EMI request 11/28



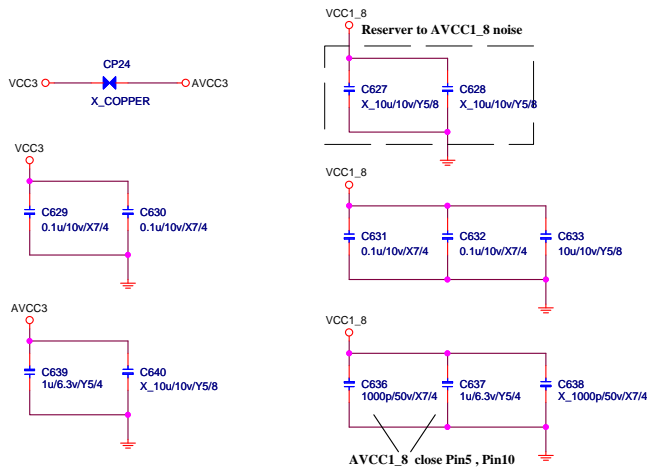
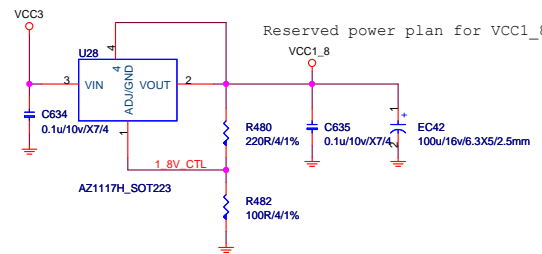
S3 Resume time

Title		
1394 Controller - JMB381		
Size	Document Number	Rev
	MS-7501	1.0
Date:	Friday, August 15, 2008	Sheet 31 of 41

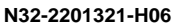
Table 5.1 JMB381 Operating Modes

	Normal	IDDQ	BIST/FL	Nandtree
XTEST	0	1	1	1
GPIO2	x	0	0	1
GPIO3	x	0	1	1

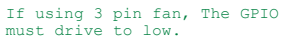
## A1117 CO-LAY SOT223 (TO\_261) PNP BJT







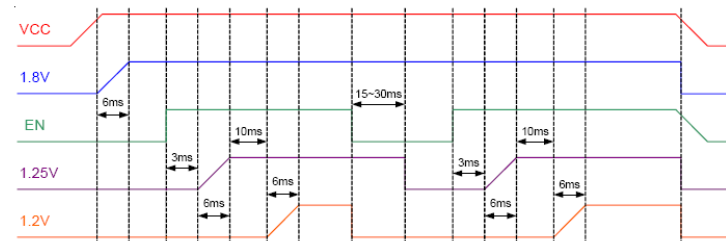
**CPU FAN**



ALL SUPPORT SMART FAN

**SYSFAN**

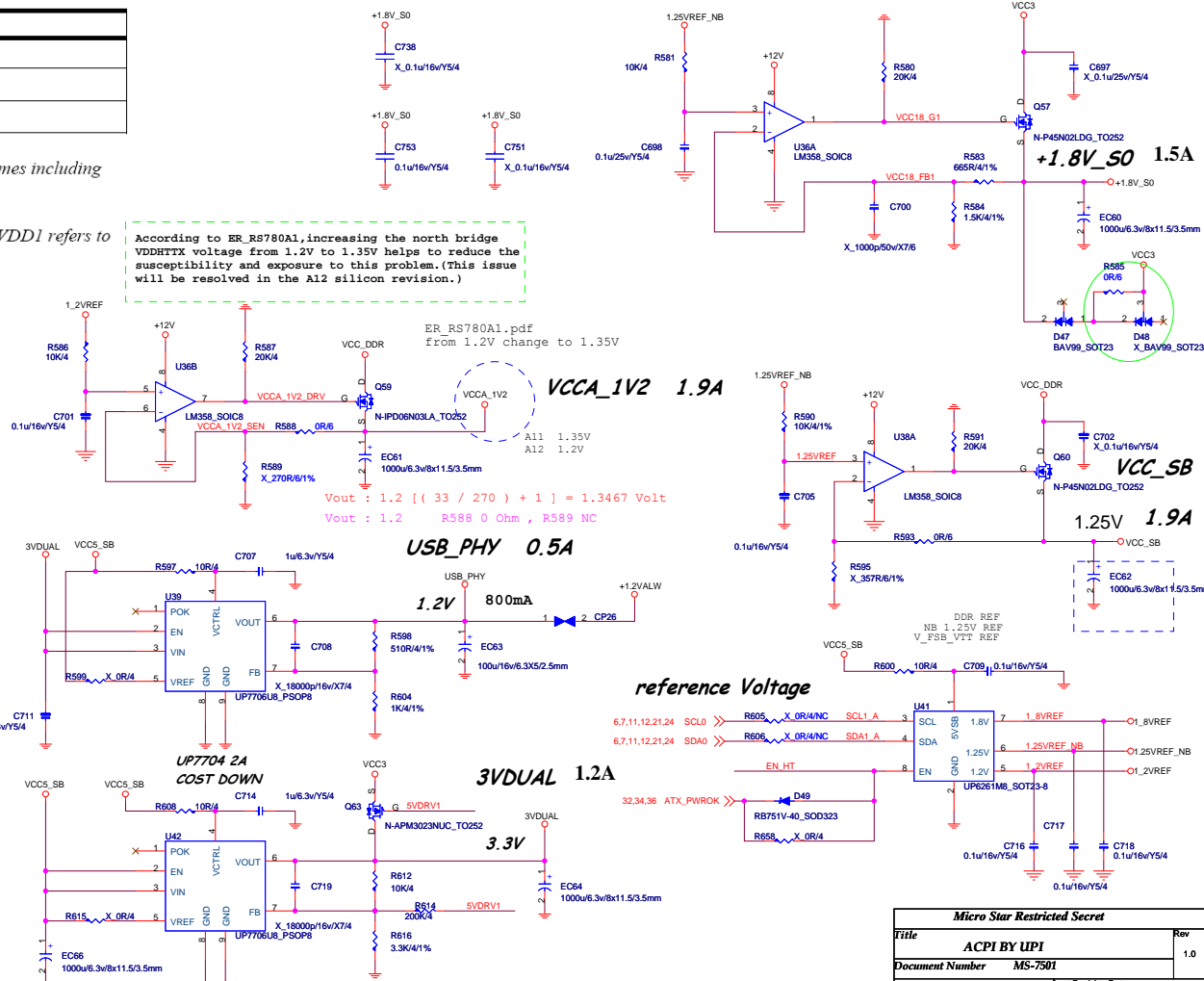
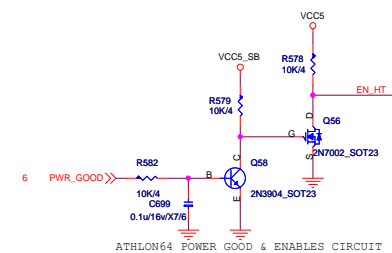
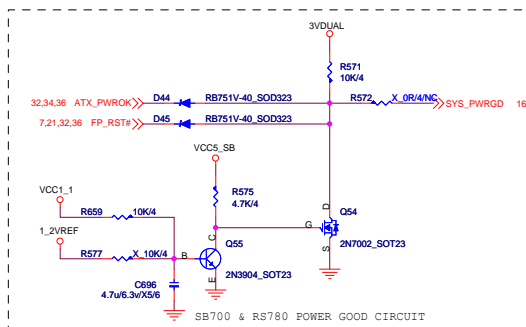
<b>Micro Star Restricted Secret</b>		
<b>Title</b>	<b>IDE Conn / FAN</b>	<b>Rev</b>
<b>Document Number</b>	<b>MS-7501</b>	1.0
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St., Jung-Hsi City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>		<b>Last Revision Date:</b> <b>Friday, August 15, 2008</b> <b>Sheet</b> 33      of      40



Note: There are no specific requirements for the following 1.1V or 1.2V rails: VDDHT, VDDHTRX, VDDHTTX, VDDPCIE

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<b>Micro Star Restricted Secret</b>		
<b>Title</b>	<b>VCC_DDR &amp; VCC1_1 NB</b>	<b>Rev</b>
<b>Document Number</b>	<b>MS-7501</b>	<b>1.0</b>
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan <a href="http://www.msi.com.tw">http://www.msi.com.tw</a>		<b>Last Revision Date:</b> <b>Friday, August 15, 2008</b> <b>Sheet</b> <b>34</b> <b>of</b> <b>40</b>

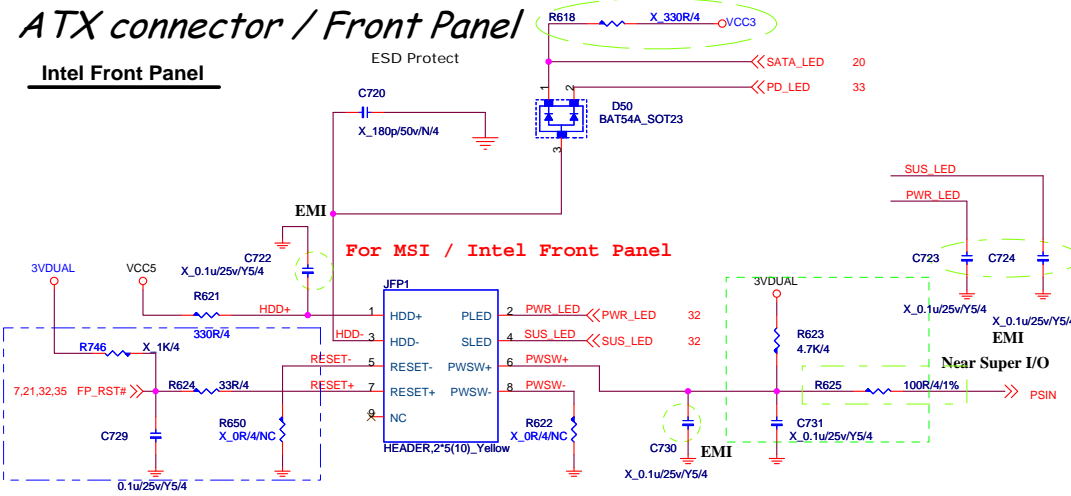


# ATX connector / Front Panel

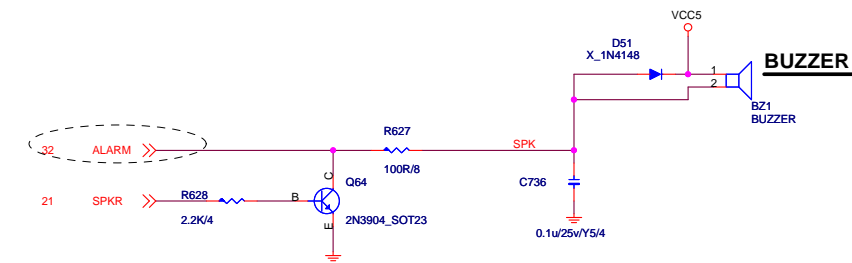
## Intel Front Panel

ESD Protect

For MSI / Intel Front Panel

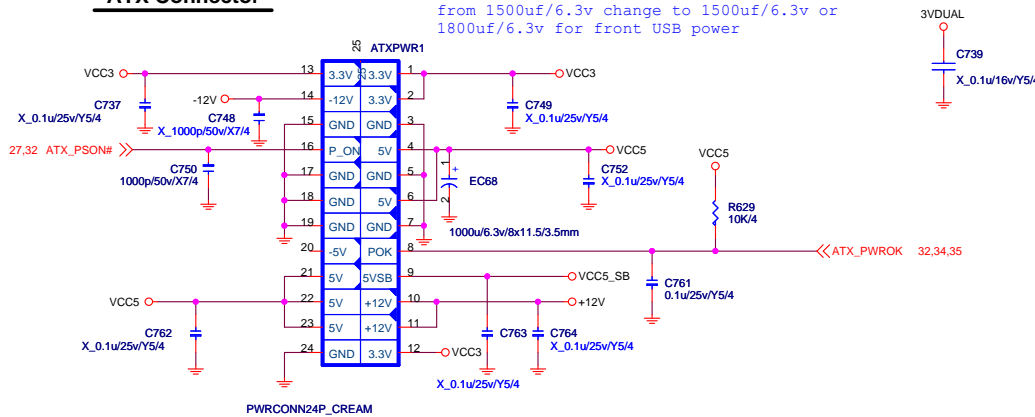


## BUZZER

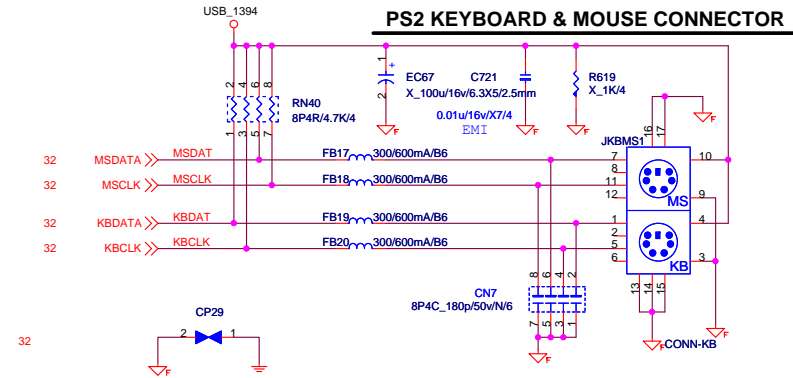


## ATX Connector

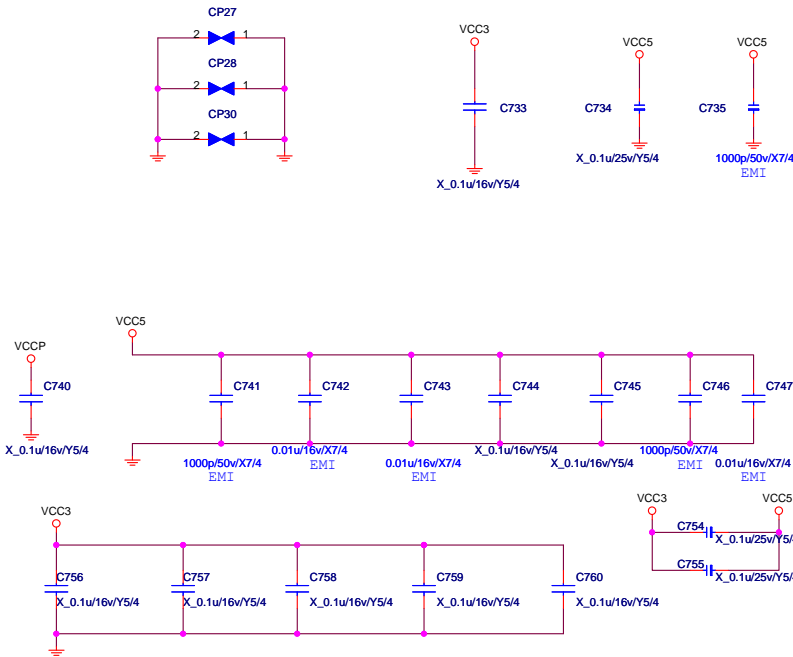
EC68 if need  
from 1500uf/6.3v change to 1500uf/6.3v or  
1800uf/6.3v for front USB power



## PS2 KEYBOARD & MOUSE CONNECTOR



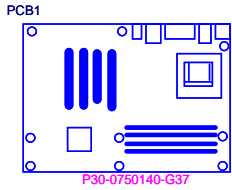
## EMI solution



Micro Star Restricted Secret		
Title	ATX/Front Panel/KB/EMI	Rev 1.0
Document Number	MS-7501	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, October 15, 2008 Sheet 36 of 40

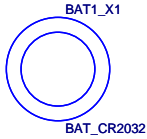


PCB

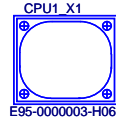


PCB : 2116  
P80-0750110-E55

BATTERY



CPU RM



LABEL



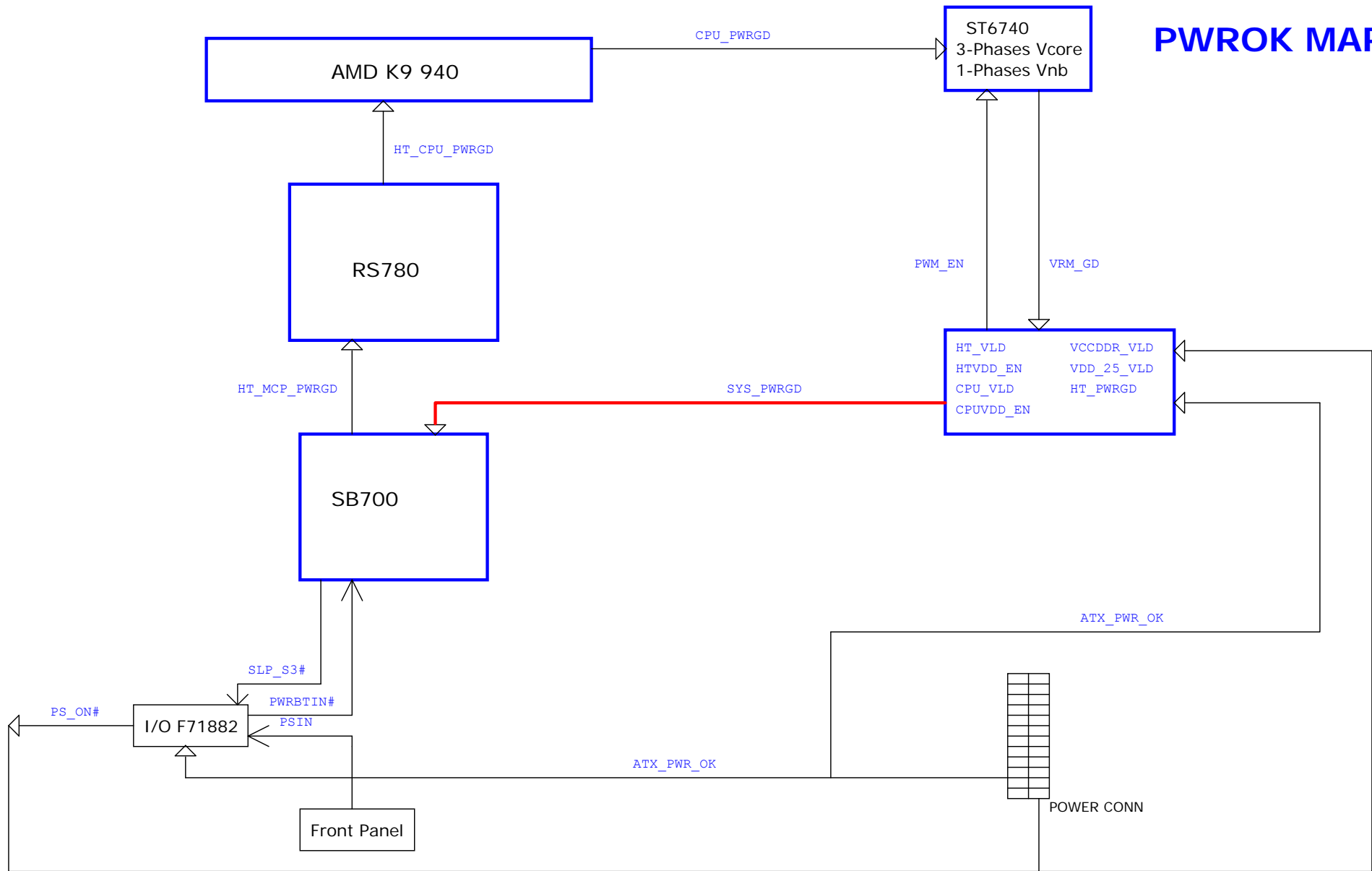
Choke9 & Choke11  
del AVL : L04-11A7031-T15  
DVI Add AVL

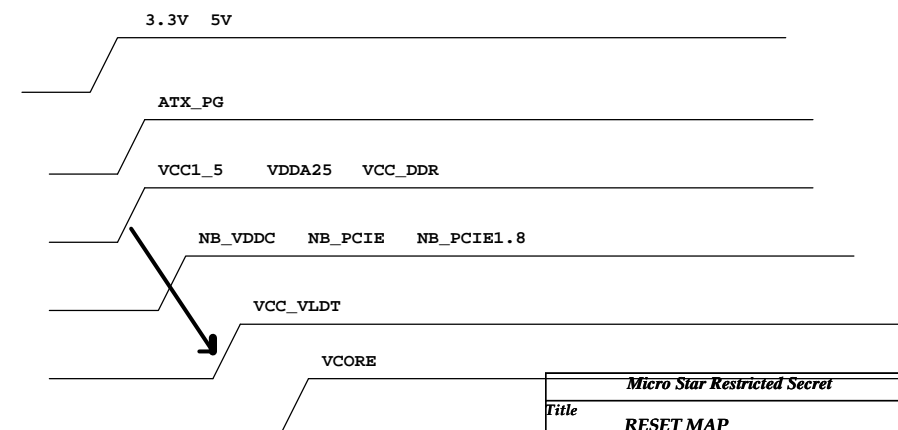
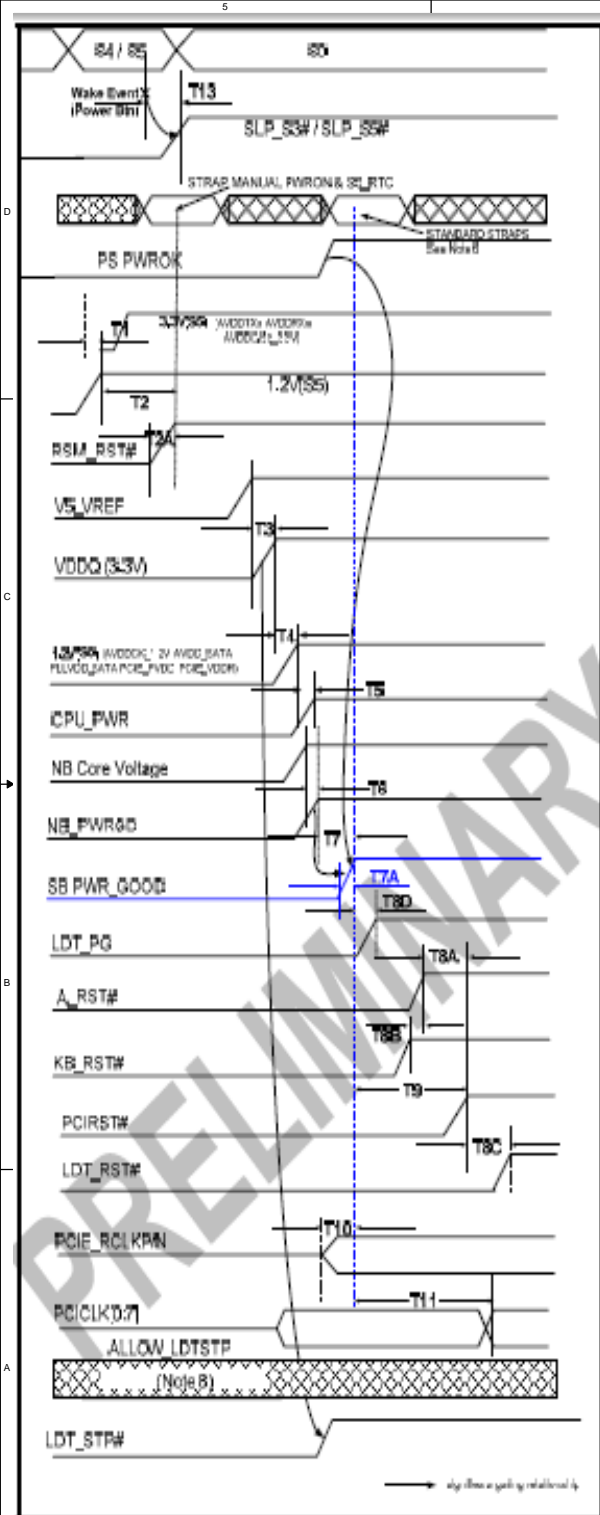
Model option table

Model type	Function	BOM Config	ERP BOM No.	OPTION
MS-7501	RS780G+SB700+HDMI ELC CAP	Cfg_HDMI	601-7501-010 (VER:A13)	A B C D E
	RS780G+SB700+DVI ELC CAP	Cfg_DVI	601-7501-020 (VER:A13)	
	RS780V+SB700+HDMI ELC CAP	Cfg_HDMI_125	601-7501-040 (VER:A13)	
	RS780V+SB700+DVI ELC CAP	Cfg_DVI_125	601-7501-030 (VER:A13)	
	RS780G+SB700+HDMI OSCON CAP	Cfg_HDMI_OSCON	601-7501-050 (VER:A13)	
	RS780G+SB700+DVI OSCON CAP	Cfg_DVI_OSCON	601-7501-060 (VER:A13)	

0512.EXP -->RS780G VER:A12 -->A13  
RS780V VER:A12 -->A13  
ADD SYSTEM SAMRT FAN FOR ALL OPTION,AND LABEL ONLY 780V

MICRO-STAR INT'L CO., LTD.			
Title BOM - Option Parts			
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- Power team Suggestion for BOM solution.
1. R40 from 19.1K change to 3K.
  2. C30 from 3.3nf change to 4.7nf.
  3. C31 from 0.022uf change to 0.1nf.
  4. R42 from 1.8K change to 820 Ohm.
  5. R76 from 34K change to 24K.
  6. R23 from 68K change to 187K.
  7. Stuff R79 5.1k.
  8. Stuff C55 220pf.
  9. Stuff R87 1K.
  10. NC C32 , R43 , R72 , R90, EC12.
  11. R699, R700, R706, R86, R88 footprint from 0402 change to NC PAD for cost down.
  12. C766, R14 NC for cost down.
  13. C16, C24, C41, C53, form Y5V change to X7R. C20, C49, C36, C6, C7, C50, C37, C21, form Y5V change to X5R.
  14. Added R761 3K pull to VCC5\_SB, R30 from 182K change to 2K. Remove R70, R36, R642, R38, R47, RT1, R75, R736, D5 Remove R12, R33, R66, R81, R8, R26, R57, R78, R10, R28, R61, R80 footprint from 0603 change to 0805. for L6740 Modulize circuit update.20071231
  15. EC1.2.3.4 change footprint to C\_P3\_5\_D8\_H20 for L6740 Modulize circuit update.20080103.
  16. NC R92 setting Upi6262 I2C address 0X60.

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1. 20071221 PM request remove DOT3 U8, R129, R131, R133, NC. Stuff R136.
2. R118, R119, R93, R94, R95, R96, R97, R98, R99, R100, R102, R103, R106, R107, R109, R110, R111, R112, R115, R117 form 0402 change to NC PAD for cost down.
3. C60 NC for cost down.
4. U7 CLKGen from Version B change to Version C.
5. C71 stuff 10pf , C72 from 10pf change to 15pf for EMI request 2007/12/20.
6. R127, R128 form 10 K change to 8.2K for 42479\_rs780\_scl\_nda\_1.01\_checklist.doc

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1. CPU pin A5 DBREQ\_L pull VCC\_DDR 300 Ohm. CPU pin AJ9 TEST22 pull down 300 Ohm. Phenom-TestNoise-Dec19-2007-MSI.pdf
2. R140, R142 from 300 Ohm change to 1K for L6740 Modulize circuit update.20080103

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1. NC C132, C133, C136, C153, C158, C159, C160 C152, C97, C100, C103, C104, C105, C108, C111 C112, C114, C115, C118, C119, C120, C127, C145, C148, Stuff C95, C117, C137, C138. for cost down.

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1. NC C220, C224, C229, C231 Stuff C217, C218, C221, C222, C223, C228, C239.

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1. Change NB hest sink part number : E31-0800590-K08.
2. Change NB Versiom A11 to A12.
3. NC C254, C255 for cost down.

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1. R176 for 4.7K Change to 330 Ohm. SB700 A12 Shiner\_Rev2.3c
2. Change R180, R185, R187, R193, R205, R209, R210 from 0402 to NC PAD for cost down.
3. NC C776, L5 & L6 added NC PAD for cost down.
4. Reserved R757, R758 for Display port.
5. Reserved C780, C781, C782 NC under NB sloder side.
6. Added R756 ; reserved R749 NC for Version A12.
7. Stuff R742, R743, R228, Remove R219, R220, Q22, R225 NC U11, R182, R226, R227, Q23, R229, R230, Q24 , R234 SB700 A12 Shiner\_Rev2.3c
8. HDMI/DVI HPD pin form TMDS\_HDP0 change to TMDS\_HPD2 follow Shiner\_Rev2.3c.
9. Remove R726 Shiner\_Rev2.3c None the resistor.
10. Q21 from 2N7002 change to N-P8503BMG.

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1. R235, R236 added NC PAD , C286, C287 NC R238 from 0402 change to NC PAD for cost down.

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1. C300, C301, C303, C319, C293, C296, C309, C310 R242, R241 Added CP52, CP51, R240 from 0402 change to NC PAD for cost down.

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1. SB change heat sink E31-0402860-K08
2. SB700 from A11 change to A12 version.
3. R244, R248, R249, R251 change to RN47. for cost down.
4. R257 L9 NC, Added CP53 for cost down.
5. R258, R259 form 0402 change to NC PAD for cost down.
6. R256 NC, SB700 A12 Shiner\_Rev2.3c

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1. SATA2 & SATA3 text change for BIOS request.
2. L10 NC added CP60, R727 NC, R270, R273 from 0402 change to NC PAD.

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1. R290 NC for A12 version.
2. R302, R303 NC follow PA\_SB600AQ2.pdf
3. R745, R285, R283 from 0402 change to NC PAD for cost down.
4. R298, R300, R304, R305 change to RN48 for cost down.
5. R306, R307, R309 change to RN41 for cost down.
6. R308, R310, change to RN42 for cost down.

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1. Remove FB10 for A12 version.
2. FB11 NC Added CP54 for cost down.
3. NC C384, C385, C390, C392, C333, C394, C396, C406, C413, C423, C427, Added C395 for cost down.

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1. Reserved R750 for display port.
2. NC R330, C433, R453, R385, R333, C472, C473, C475, C457, C458, C460, Q75, R58, Q74, Q71, R657, Q70, Q72, Q73 for cost down.

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1. IDSEL1/2 form AD18/AD19 change to AD21/AD22 follow Shiner\_Rev2.3c
2. NC C478, C479, C484, C480, C482, C488, C483, C486, Stuff C489 for cost down.

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1. NC C769, C772, C770, C771, C773, for cost down.
2. Stuff L19, L21 90 Ohm common chock for EMI request 2007/12/20.
3. Remove R487, R558, R485, R488, Q34, Reserved R762, C785 Added R765, R764, R763, Q81, Q82, for USB power enabled control.

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1. Remove L30, L31, NC D17, D18 for cost down.
2. NC R347, R352, Q26, Q27, Stuff R351, R354 R348, R349 connect to 5V\_VGA.
3. R339, R340, R341 from 150 Ohm change to 120 Ohm. NC C495, C497, C500, C496, C498, C501 from 5pf change to 1.8pf. for signal quality.

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1. Reserved R766, R767, R768, R769, R770, R771, R772, R773 for EMI request 20080104.
2. R362, R364, R367, R372, R376, R379, R382, R384 from 18 Ohm change to 0 Ohm follow Shiner\_Rev2.3c
3. Remove L36, L37 Added R760 for HOT\_DET pin.
4. R366, R371 from 15k Ohm change to 6.8K Ohm. follow Shiner\_Rev2.3c.
5. HOT\_DET pin from TMDS\_HPD0 change to TMDS\_HPD2 follow Shiner\_Rev2.3c.
6. Reserved EC75, Added D53 1N5817. NC C524.
7. R370, R374 from 0402 change to NC PAD for cost down.
8. NC Q30, Q31, Stuff R368, R375 follow Shiner\_Rev2.3c.

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1. C549, C550 from 0.1uf change to 0.22uf RealTek suggestion.
2. NC C547, C553, C557, C544, R409 from 0402 change to NC PAD.
3. NC U23, C530, R397 EEPROM less for cost down.
4. LAN connector change P/N N58-22F0631-F02 for EMI request.

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1. R416 from 0402 change to NC PAD. R428, R429, R430 change to RN45. R433, R434, R435 change to RN46. for cost down.

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1. R461, R462, R463, R465 change to RN43. R472, R474, R475, R477 change to RN44 for cost down.

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1. R490, R494 from 0402 change to NC PAD NC R507, Q36 for cost down.
2. R687, R689 for cost down. BIOS request : R685 for DVI detection. R686 for HDMI detection.

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1. R530 from 200k change to 200 Ohm BOM error.
2. C655 from 0.1uf/25v/Y5V change to 01.uf/50V/ X7R C657 from 0.1uf/50v/Y5V change to 01.uf/50V/ X7R
3. NC C653 , C659 , EC44 for cost down.
4. EC43, EC44 from 100u/16v/6.3x5/2.5mm change to 100u/25v/6.3x11/2.5mm
5. Modify MH1 , MH2 added CP57, CP58 , MH4 Added CP59 for EMI request 20071225.

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1. Choke9 & 11 remove AVL L04-11A7031-T15 footprint issue.
2. NC R545, Stuff R544, Added R752, R751, Q78, Q77 Reserved C783 for meet power rail power-up sequence.
3. Remove EC54, NC R741, C684, C683, C665, EC59, EC58 from 1000uf change to 1800uf, R696, Added CP55, CP56 for cost down.
4. Remove R698 for L6740 Modulize circuit update.20080103.
5. Remove C660, U32, R539, R541, C661, C662, C663 NB A12 not need.

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1. Added R753, R755, R754, Q80, C784, Q79, Patch COOLERMASTER 700W POWER Sequence
2. R572, R605, R606 form 0402 change to NC PAD NC EC65 for cost down.
3. Stuff R610, NC R607 change mode.
4. Stuff R585 follow Shiner\_Rev2.3c.
5. NC R589, R588 from 33 Ohm change to 0 Ohm for NB A12.

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1. Stuff C721, C735, C741, C742, C743, C746, C747 for EMI request 2007/12/20.
2. C725, C726, C727, C728 change to CN7 for cost down.
3. NC R618 , R618 from 3VDUAL change to VCC3.
4. R621 from 33 Ohm change to 330 Ohm. BOM error.
5. R650, R622 form 0402 change to NC PAD for cost down.
6. Remove R620, R626.
7. Reserved R746 for FP\_RST#.
8. NC C749, C748, C752, C763, C764 for cost down.

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1. R23 => 56K, R40 => 4.99K, C30 => 3.3nF, C32 => 6.8nF R43 => 100R, R90 => 0R
2. Remove C55, R87, EC6, EC8

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1. R718, R719, R720, R721, R722, R723, R724, R725 from 4.99 Ohm change to 0 Ohm follow Ap\_note AN\_SB700AB5

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